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Depleted Monolithic Active Pixel Sensors (DMAPS)

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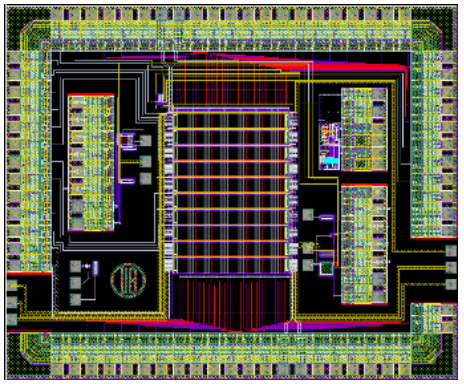
Who am I?

2013

PhD in Engineering and Advanced Technologies @ University of Barcelona

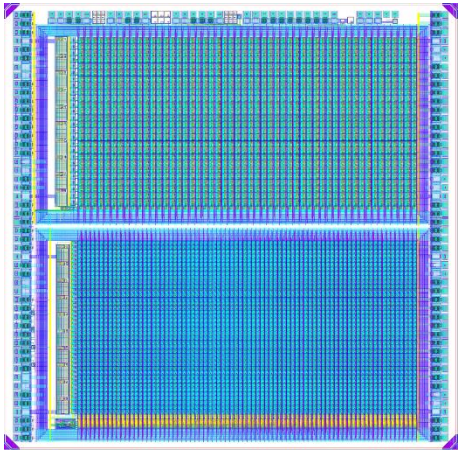
- Prototype detector for possible future linear colliders
- Application in medical devices



2014 to 2019

PDRA @ University of Liverpool

- New R&D programme to develop DMAPS for particle physics experiments
- Prototype detectors for ATLAS and Mu3e with international collaborations
- More generic developments with the CERN-RD50 collaboration



2019

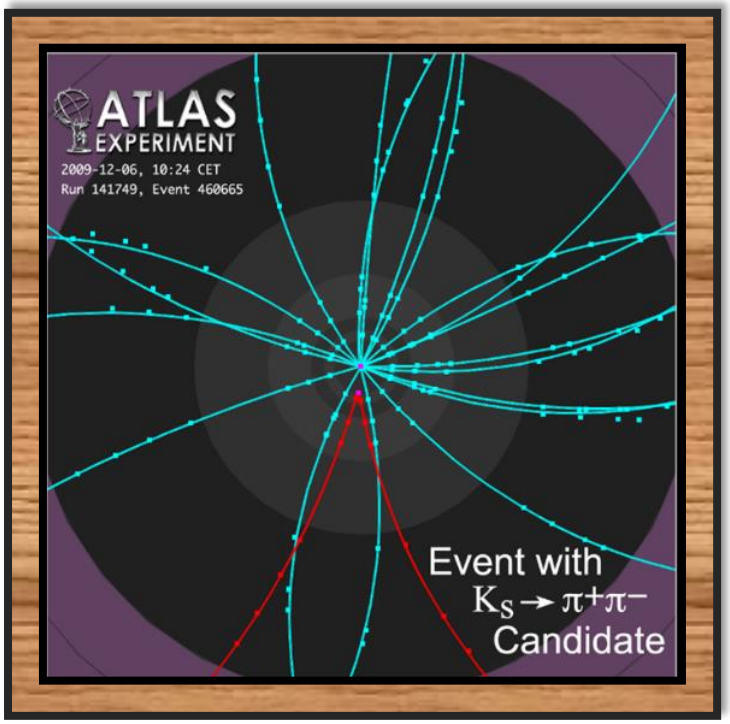
UKRI Future Leaders Fellow @ University of Liverpool

- Established R&D programme to develop highly performant DMAPS for future particle physics experiments
- Group leader of the Liverpool DMAPS R&D programme
- Member of several international collaborations (CERN-RD50, LHCb, etc.)

Outline

- **Silicon tracking detectors**
  - Sensor detection principle
  - Readout electronics
- **Pixels**
  - Hybrids
  - Monolithic Active Pixel Sensors – MAPS
  - Depleted Monolithic Active Pixel Sensors – DMAPS
    - Commercial vendors
    - Low vs large fill-factor
- **DMAPS for particle physics**
  - Mu3e
  - ATLAS ITk upgrade
  - CERN-RD50
    - Main design aspects
    - Main evaluation results
- **Conclusion**

Particle tracking



Silicon tracking detectors – Specifications

Dear Santa,

Here is my wish

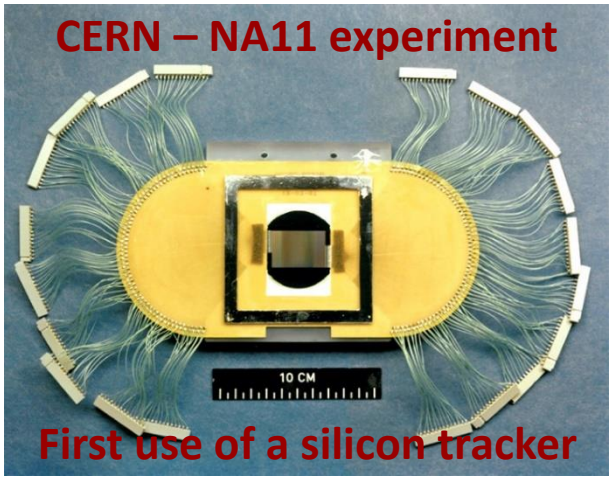
Pixel size	→	small (a few μm^2)
Radiation tolerance	→	high (> 10^{17} 1MeV n_{eq}/cm^2)
Time resolution	→	excellent (< 100 ps)
Material budget	→	minimal (< 50 μm)
Power consumption	→	minimal (~10-100/cm^2)
Noise	→	minimal
Reticle size	→	large
Assembly process	→	as easy as possible
Yield	→	high (and cheap price!!!)

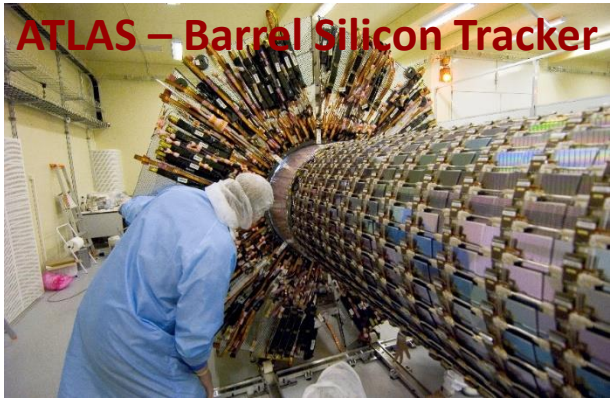
Love,

The physicists

Silicon tracking detectors

- Silicon tracking detectors have been used in particle physics experiments since the early 80's
- They introduced a significant improvement of the spatial resolution in comparison to that provided by state-of-the-art detectors at the time:
  - Multi-wire proportional chambers (< 1 mm)
  - Drift chambers (~100 µm)
- Two main variants:
  - **Micro-strips** (~10 µm spatial resolution)
    - 100 channels/cm^2
  - **Pixels** (~10 µm spatial resolution)
    - 5000 channels/cm^2
    - True 3D reconstruction
    - Capable to cope with high density and rate particle tracks
    - Capable to survive harsh radiation environments
      - ➔ Close to the interaction point



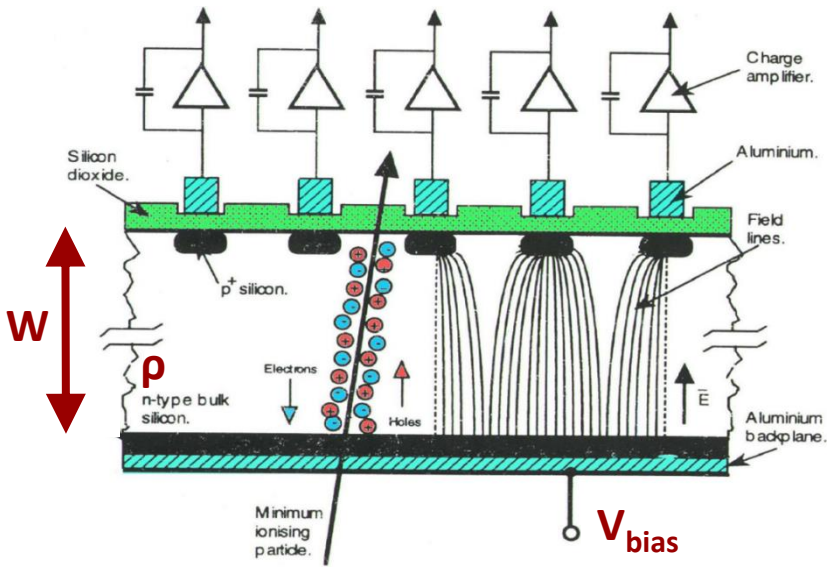


CERN server

Sensor – Detection principle

- Silicon p-n diode in reverse bias
- A traversing particle creates e^-/h^+ pairs by ionization
- The electric field separates the e^-/h^+ pairs, which move to the detector electrodes where they generate signal
- Basic requirements:
  - **Large bias voltage (V_{bias})**
    - Larger W → larger signal
    - Faster charge collection
    - Better radiation tolerance
  - **High resistivity silicon bulk (ρ)**
  - **Backside biasing**
    - More uniform electric field lines
    - Improved charge collection efficiency

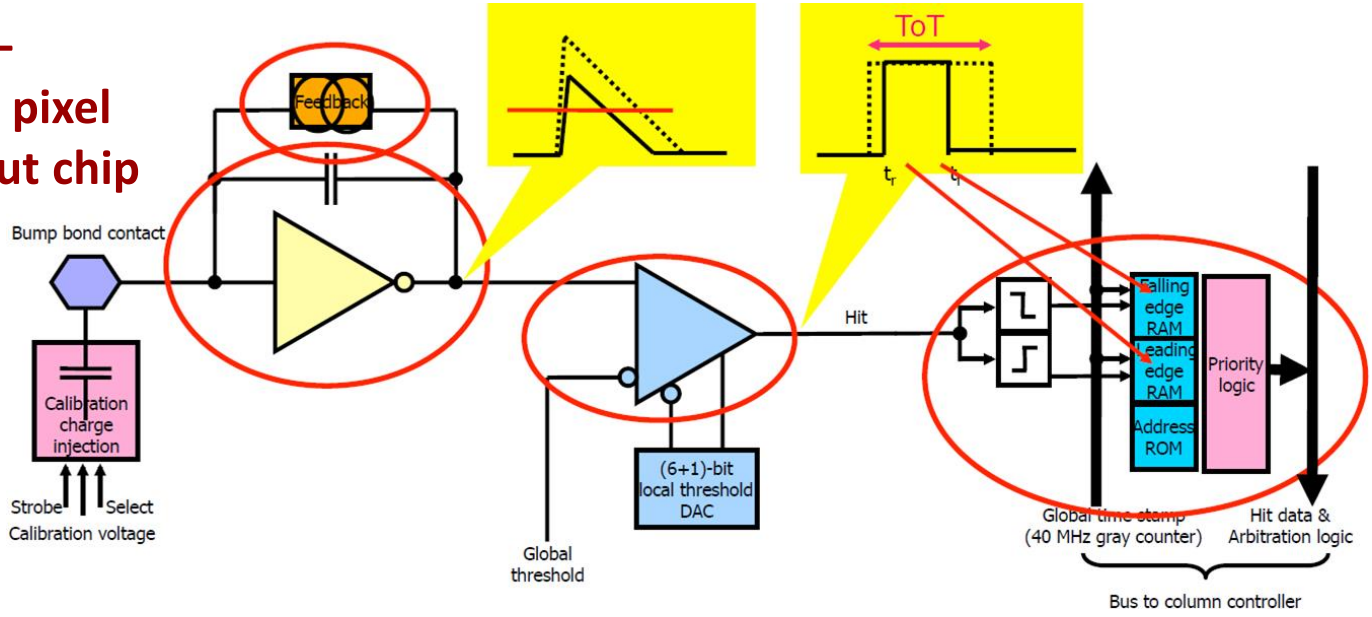
→ $W = \sqrt{\rho \cdot V_{bias}}$



- The signal is amplified, discriminated and digitized by the readout electronics

Readout electronics – Block diagram

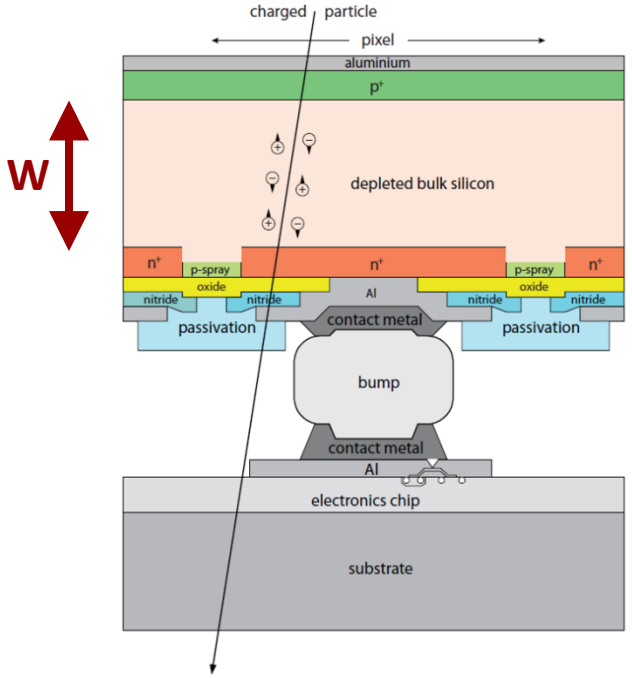
FE-I3 – ATLAS pixel readout chip

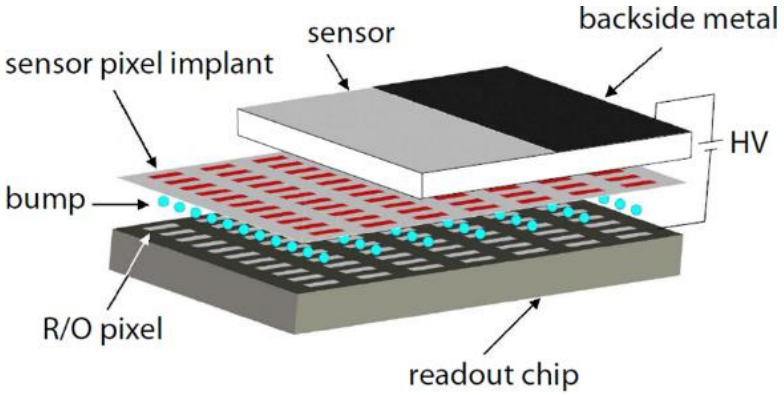


- **Charge Sensitive Amplifier (CSA)**
  - Signal charge integration
  - Pulse shaping (feedback capacitor with constant current)
- **Comparator with DAC for local threshold voltage compensation**
  - Pulse digitization
  - Length of digital pulse determined by time at which the rising and falling edges cross the comparator threshold voltage (Time over Threshold or ToT)
- **RAM and ROM memories** to store time-stamps and pixel address
- In deep sub-micron technologies for high density of integration

Hybrid pixel detectors

- Sensor and readout electronics on separate wafers
- **Best technology for the sensor and the readout electronics**
  - Very fast charge collection by drift (1 ns)
  - Fully depleted bulk (large signal)
  - Radiation tolerant (10^{16} 1MeV n_{eq}/cm^2)
  - Capability to cope with high data rates
- **1-to-1 connection between sensor and readout chip via tiny conductive bumps using bumping and flip-chip technology**
  - Limited pixel size (55 µm x 55 µm)
  - Substantial material thickness (300 µm)
  - Limited fabrication rate (bump-bonding and flip chipping is complex)
  - Expensive (> £1M/m^2) – custom wafers and processing
- **State-of-the-art for high rate experiments**

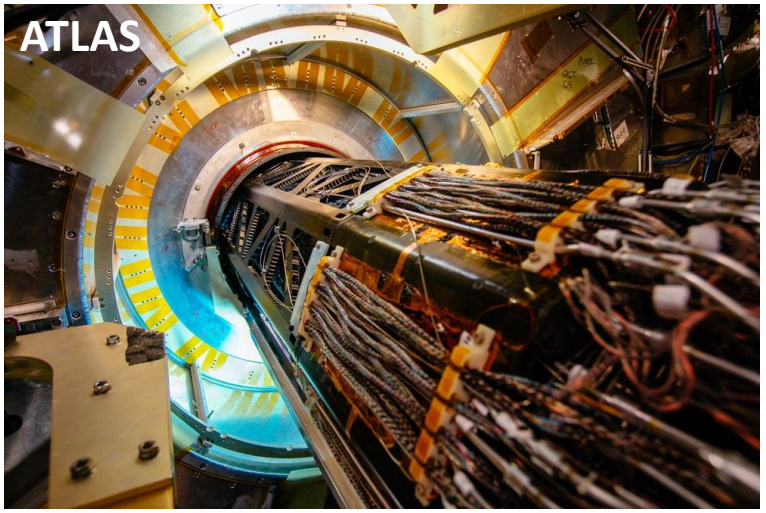


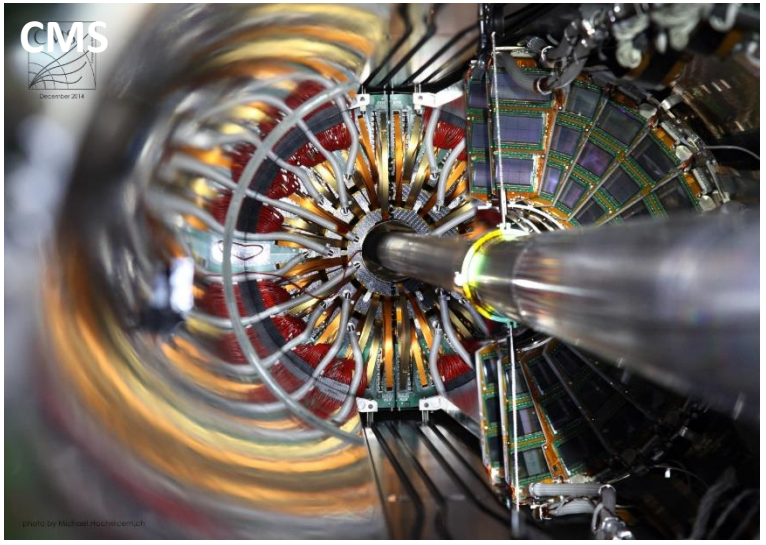


M. Garcia-Sciveres, arXiv:1705.10150v3, 2018

Hybrid pixel detectors in HEP

- **ATLAS, CMS and ALICE** use hybrid pixel detectors near the interaction point
- Complemented by hybrid strip detectors at larger radii
- Largest detector systems ever built in HEP (several m^2)

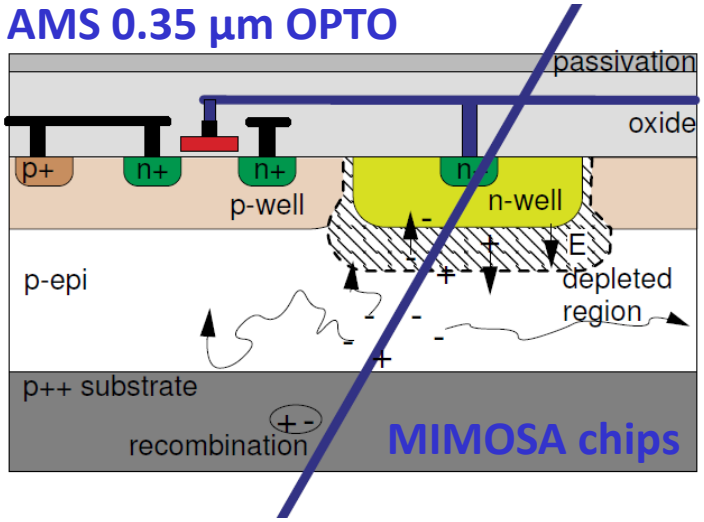




Monolithic pixel detectors – MAPS

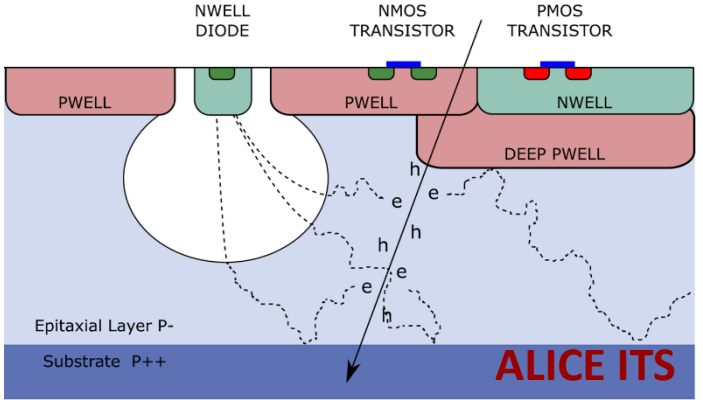
- Sensor and readout electronics on single wafer in standard CMOS (low-voltage CMOS)
  - Reduced material thickness (50 µm)
  - Small pixel size (18 µm x 18 µm)
  - In-pixel signal amplification
  - More cost effective (~£100k/m^2)
  - Small bias voltage (V_{bias})
    - Slow charge collection by diffusion (2 µs)
    - Limited radiation tolerance (10^{13} 1MeV n_{eq}/cm^2)
- **State-of-the-art for high precision experiments**

AMS 0.35 µm OPTO



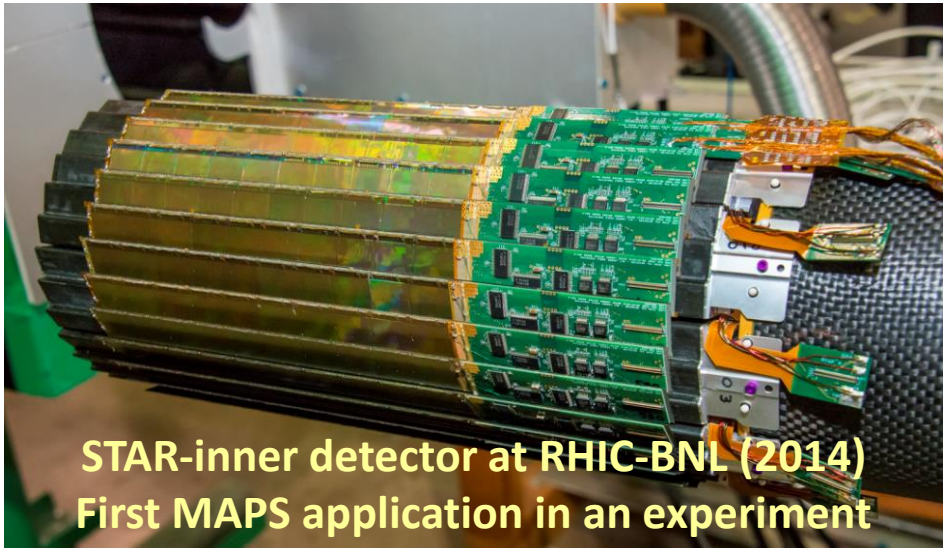
Pixel = Sensor + simple amplifier

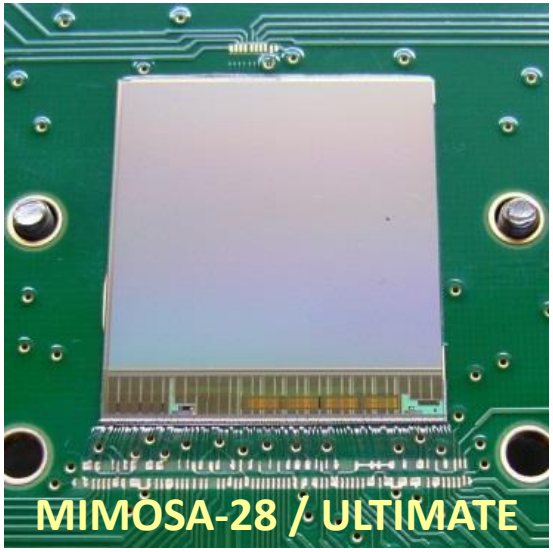
TowerJazz 180 nm



Pixel = Sensor + complex electronics

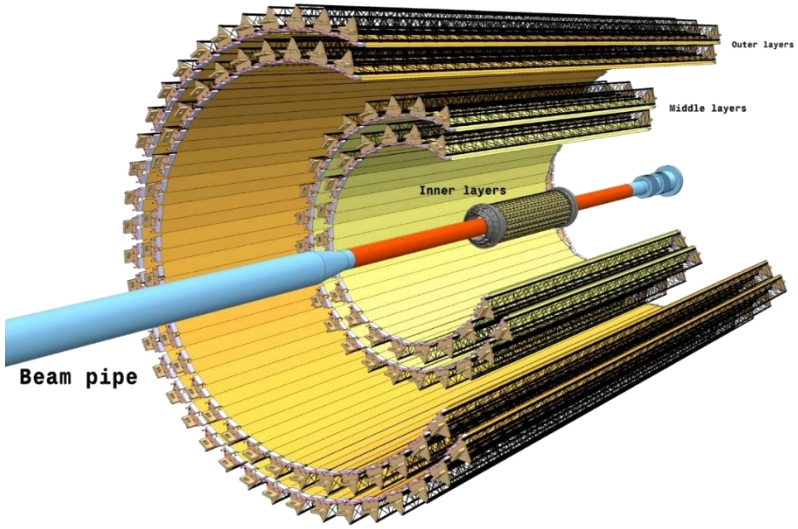
MAPS in HEP (I)





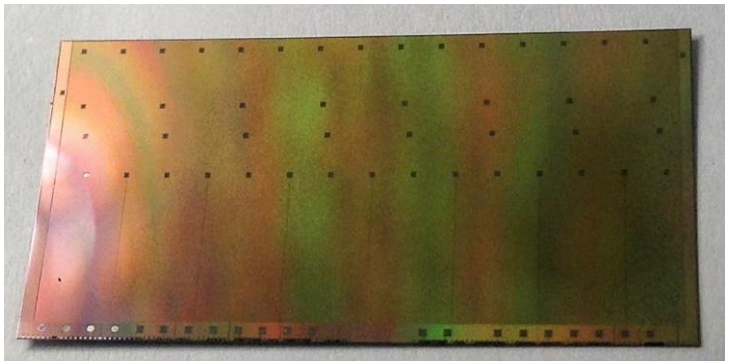
- **MIMOSA-28 / ULTIMATE chip:**
  - Chip size — 20 mm x 22 mm
  - Total detector area — 0.15 m^2
  - Sensor matrix — 928 x 960 pixels (~0.9 Mpixels)
  - Pixel size — 20.7 µm x 20.7 µm
  - Radiation tolerance — 150 krad (TID)
    10^{12} 1 MeV n_{eq}/cm^2 (NIEL)
  - Process — AMS 0.35 µm OPTO

MAPS in HEP (II)



ALICE ITS upgrade (2020)

M. Mager, NIM-A: 824 434-438, 2016

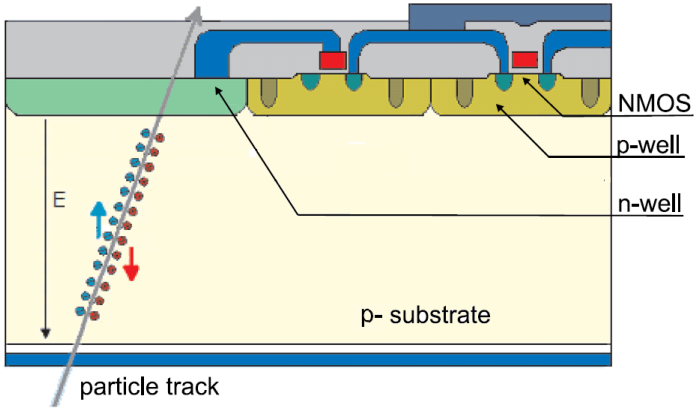


ALPIDE

- **ALPIDE chip:**
  - Chip size — 15 mm x 30 mm
  - Total detector area — 12 m^2
  - Sensor matrix — 512 x 1024 pixels (> 0.5 Mpixels)
  - Pixel size — 28 µm x 28 µm
  - Radiation tolerance — 700 krad (TID)
    10^{13} 1 MeV n_{eq}/cm^2 (NIEL)
  - Process — TowerJazz 180 nm

Monolithic pixel detectors – Depleted MAPS

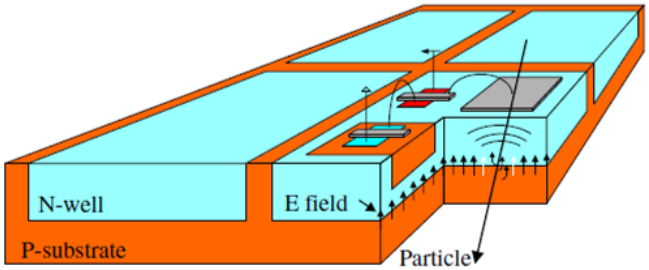
- Sensor and readout electronics on single wafer in standard High Resistivity/High Voltage-CMOS (HR/HV-CMOS)
  - Reduced material thickness (50 µm)
  - Small pixel size (50 µm x 50 µm)
  - In-pixel amplification
  - More cost effective (~£100k/m^2)
  - Larger bias voltage (V_{bias})
    - Fast charge collection by drift (15 ns time resolution)
    - Good radiation tolerance (10^{15} 1MeV n_{eq}/cm^2)
  - One limitation: The chip size is in principle limited to 2 cm x 2 cm, although stitching options are being investigated



- **Next generation**

DMAPS – History

- HV-CMOS processes originally used for driving automotive or industrial devices
- 2007 → First publication of a HV-CMOS detector chip (test chip in 0.35 µm HV-CMOS process from AMS)
  - Small pixel matrix
  - Pixels = Sensor + pixel electronics (CSA, discriminator and digital storage)
  - Pixel electronics in the deep n-well
  - Successful measurements with X-ray and beta radioactive sources
  - HV contacts at the top side
- HV-CMOS processes are attractive for particle physics because
  - Silicon bulk biased at high voltage (e.g. -100 V)
  - Multiple nested wells to isolate the low-voltage CMOS readout electronics from the bulk
  - Commercially available (i.e. fabrication is low-cost and reliable, there is availability of multiple vendors and large scale production)



I. Peric, NIM-A: 582 876-885, 2007

DMAPS – Commercial vendors (I)

TSI SEMICONDUCTORS

GLOBALFOUNDRIES

DMAPS – Commercial vendors (II)

Foundry → / Parameter ↓	LFOUNDRY A SMIC COMPANY	TOWERJAZZ The Global Specialty Foundry Leader	TSI SEMICONDUCTORS
Feature node	150 nm	180 nm	180 nm
HV	Yes	No	Yes
HR	Yes	Yes	Yes
Quadruple well	Yes	Yes	No (triple)
Metal layers	6	6	6
Backside processing	Yes	Yes	No
Stitching	Yes	Yes	Yes
TSV	No	No	–

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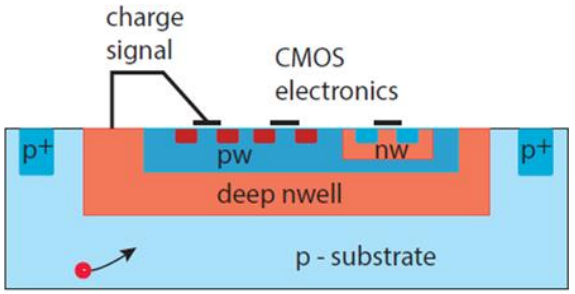
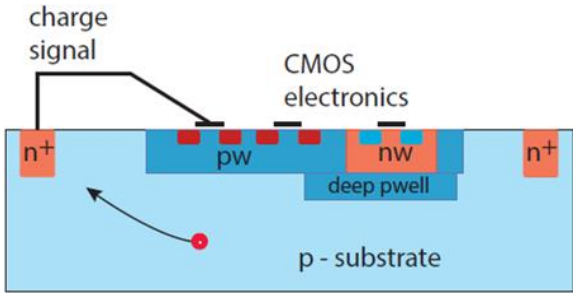
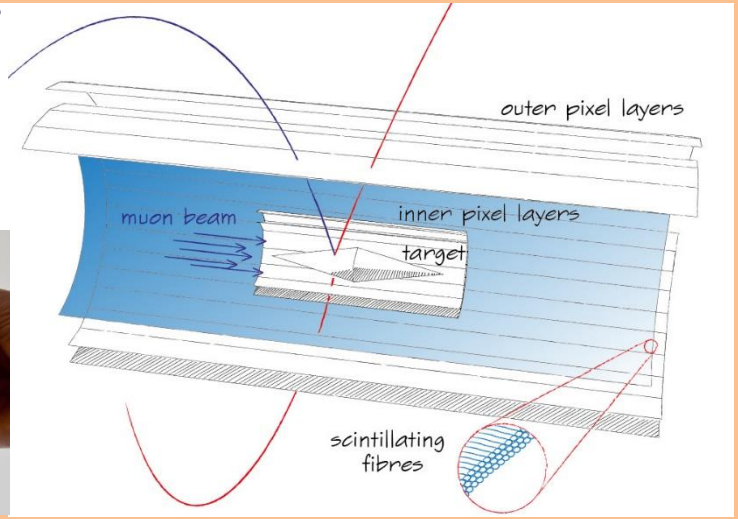
DMAPS – Large vs small fill-factor

Sensor cross-section → **Parameter ↓**		
Name	Large fill-factor (HV/HR-CMOS)	Small fill-factor (HR-CMOS)
1) p/n junction	p-substrate/large deep n-well	p-substrate/small shallow n-well
2) Substrate biasing	High voltage	Low voltage
3) Substrate resistivity	< 2-3 kΩ·cm	< 8 kΩ·cm
1) + 2) + 3)	▪ No (little) low-field regions ▪ Shorter drift distances ▪ Higher radiation tolerance ▪ Larger sensor capacitance ▪ Larger noise & speed/power penalties ▪ RO in charge collection well	▪ Low-field regions ▪ Longer drift distances ▪ Lower radiation tolerance ▪ Very small sensor capacitance ▪ Reduced noise & power ▪ RO outside charge collection well
Process	AMS/TSI and LFoundry	TowerJazz

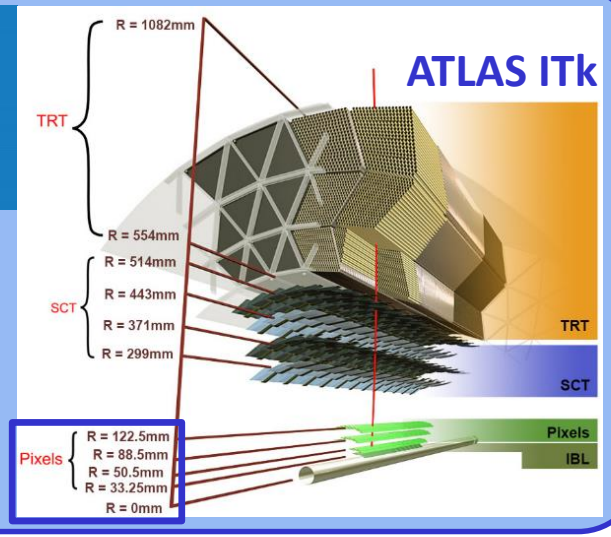
DMAPS in HEP



- **First DMAPS application in an experiment (2019+)**
- Requirements:
  - Low material
    50 µm
  - Good time resolution
    < 20 ns (for pixels)
  - Fine segmentation
    80 µm x 80 µm

ATLAS EXPERIMENT

Cancelled



LHCb

2024
2030

CLIC

2035+

RD50

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Mu3e – Pixel detector history

Prototype	Year	Active area (mm^2)	Functionality	Main features
MuPix1	2011	1.77	Sensor + analog RO	First MuPix prototype
MuPix2	2011	1.77	Sensor + analog RO	
MuPix3	2012	9.42	Sensor + analog/digital RO	First digital RO
MuPix4	2013	9.42	Sensor + analog/digital RO	Working digital RO and time-stamping
MuPix6	2013	10.55	Sensor + analog/digital RO	
MuPix7	2014	10.55	SoC (all relevant features for a fully monolithic chip)	First MuPix prototype with state machine, clock generation and fast serial RO (1.25 Gbit/s)
MuPix8	2017	160	Large SoC	First large MuPix prototype, with TW correction
MuPix9	2018	17.2	SoC	Voltage regulators
MuPix10	2019	479	Full size (reticle) SoC	First full size SoC

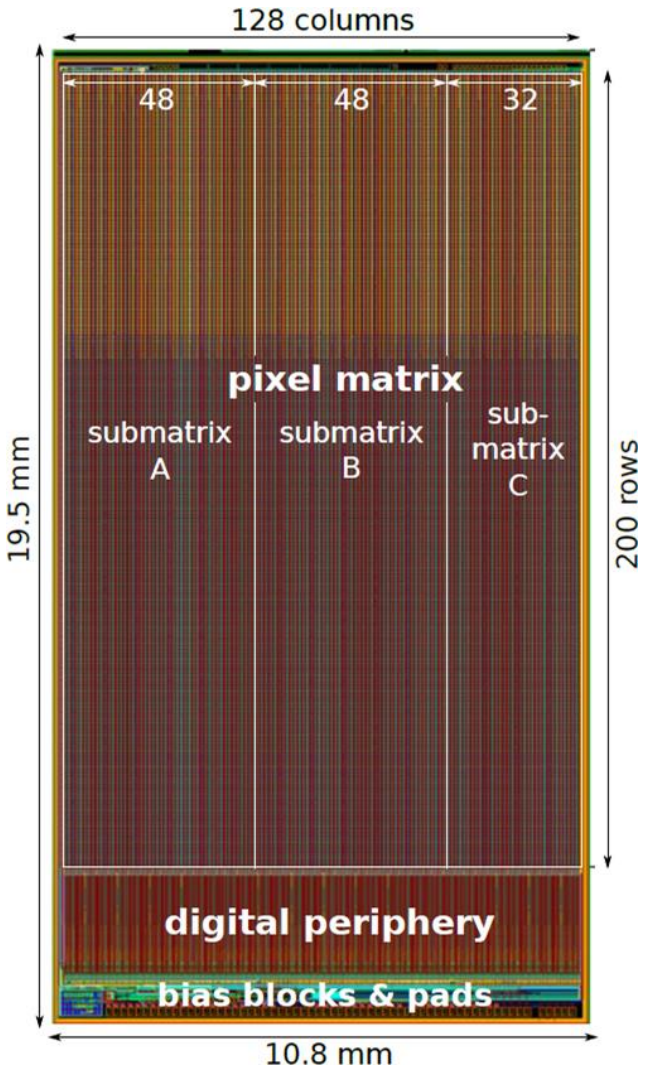
Mu3e – MuPix8

MuPix8 - General design features

- Engineering run in the **180 nm HV-CMOS process from ams (aH18)**
- Shared with ATLASPix1 (MuPix8 is ~1 cm x 2 cm)
- Fabricated in 2017
- Fabricated using 3 different substrate resistivities
  - 10 Ω·cm, 50-100 Ω·cm and 100-400 Ω·cm

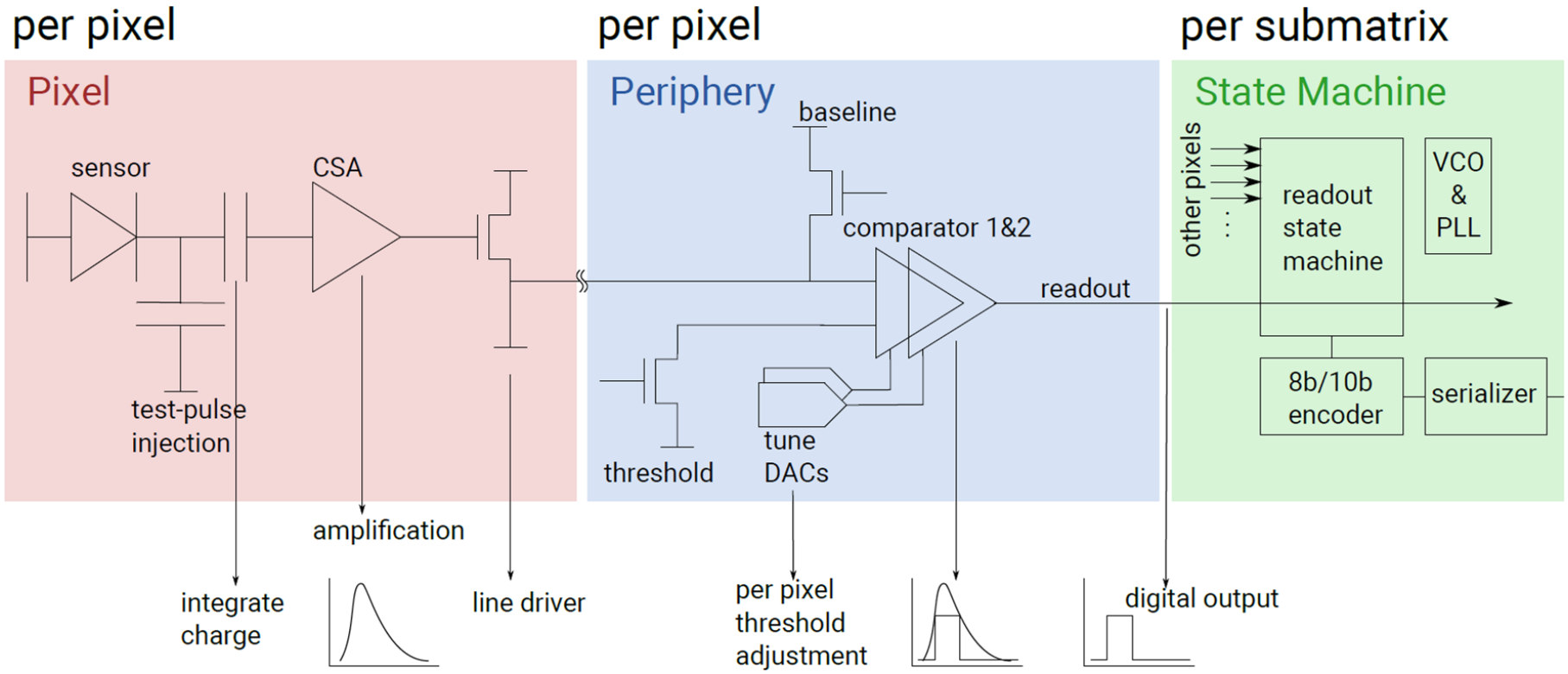
MuPix8 – Chip details

- Matrix with 128 columns x 200 rows
- 3 matrix partitions (sub-matrices A, B and C)
- 81 µm x 80 µm pixel size
- Analog readout in pixel cell
  - Charge sensitive amplifier
- Digital readout in periphery
  - Discriminator
  - 6-bit ToT
  - State machine (continuous readout)
- Time-walk reduction circuitry
- Serial links < 1.6 Gbit/s
- Power consumption ~250 mW/cm^2



J. Kroeger, MSc thesis Uni. Heidelberg, 2017

Functional block diagram of the chip architecture



H. Augustin, arXiv:1905.09309v1, 2019

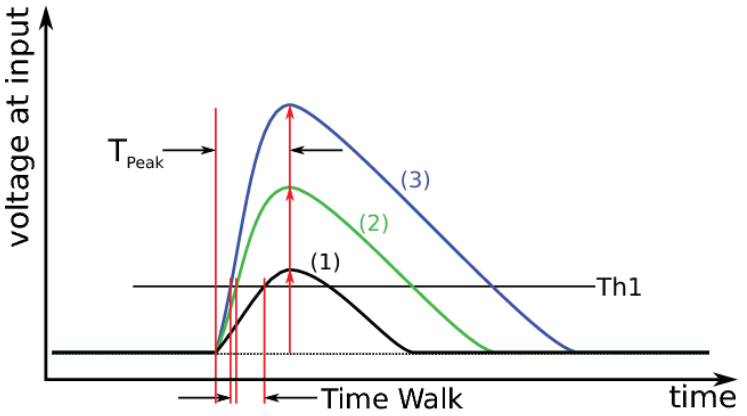
Mu3e – Time-walk correction

Time-Walk (TW)

- What is it? Variation of the response time of the readout electronics depending on the number of e^-/h^+ pairs collected by the sensor

TW correction – Two-threshold method

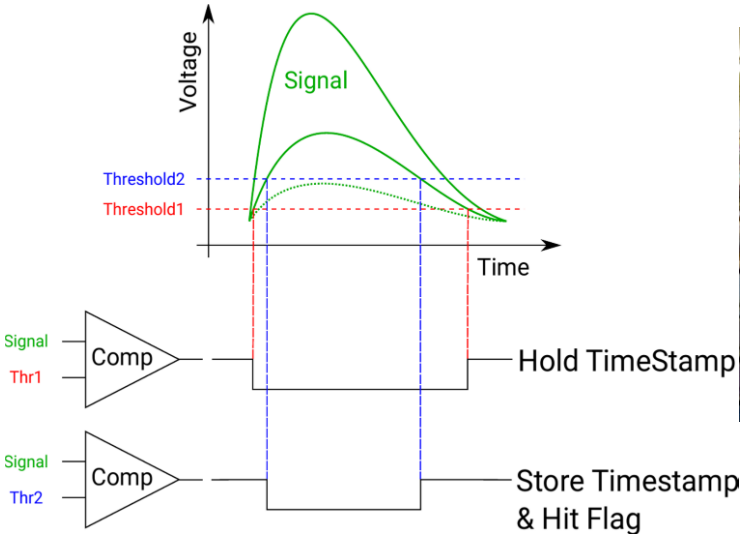
- Two comparators with two threshold voltages:
  - VTH1 is very low (close to the noise level) → it delivers a time-stamp with small TW
  - VTH2 > VHT1 → it confirms that the flagged time-stamp corresponds to a real signal and not to noise
- Measured results show the TW can be reduced to ~6 ns



R. Schimassek, IEEE NSS/MIC/RTSD, 2016

TW correction – Other methods

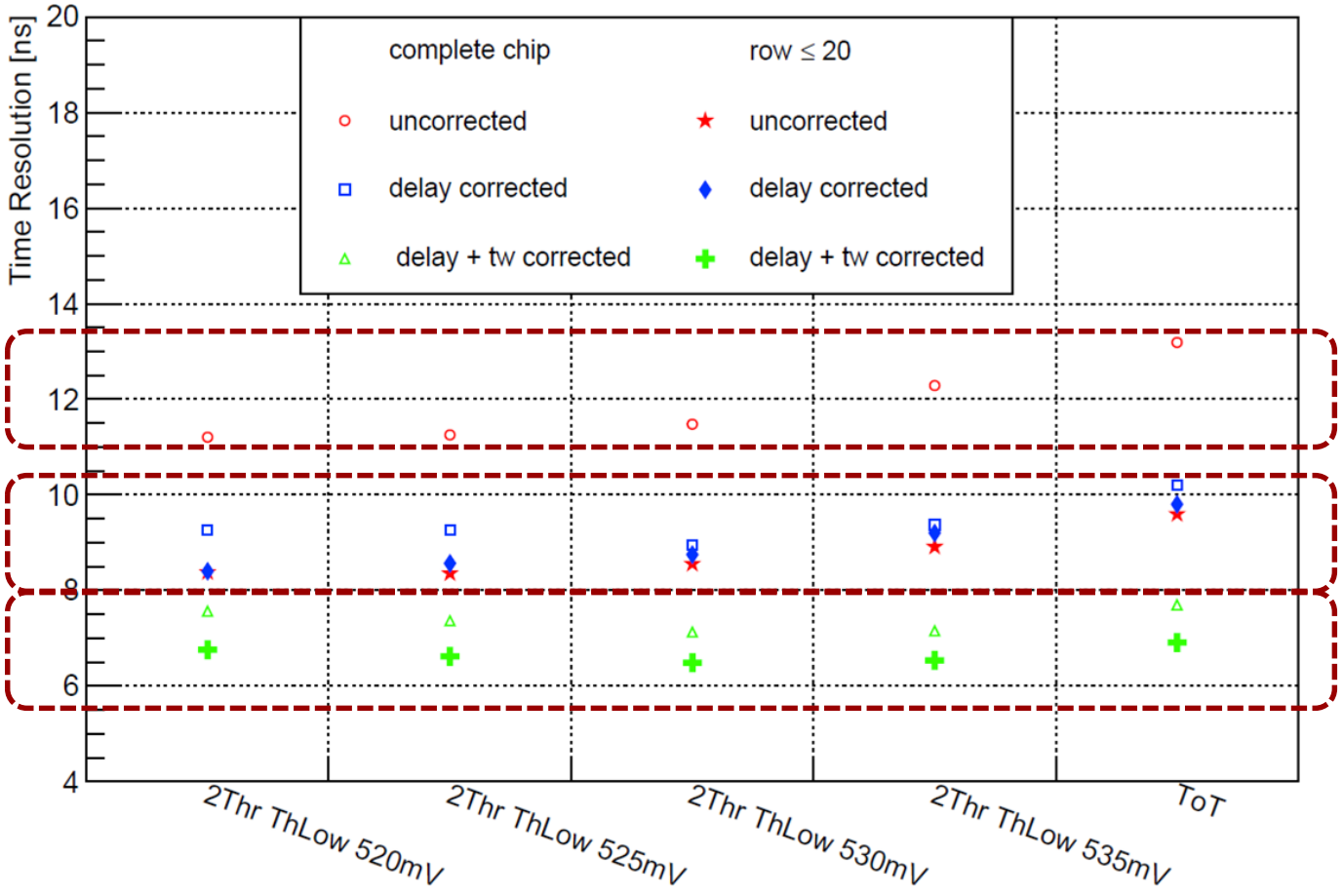
- Increasing the response rate of the amplifier (CACTUS, RD50-MPW2)
- Time-walk compensated comparator (HVStripV1, H35DEMO)
- Sampling method (LF-ATLASPix, CERN-RD50)



H. Augustin, PoS (VERTEX2017) 057

Mu3e – Time resolution

- Measurement with MuPix8 + scintillator and a Sr90 source
- Time resolution = Time difference between the hit on MuPix8 and scintillator



Matrix level
σ = 14 ns

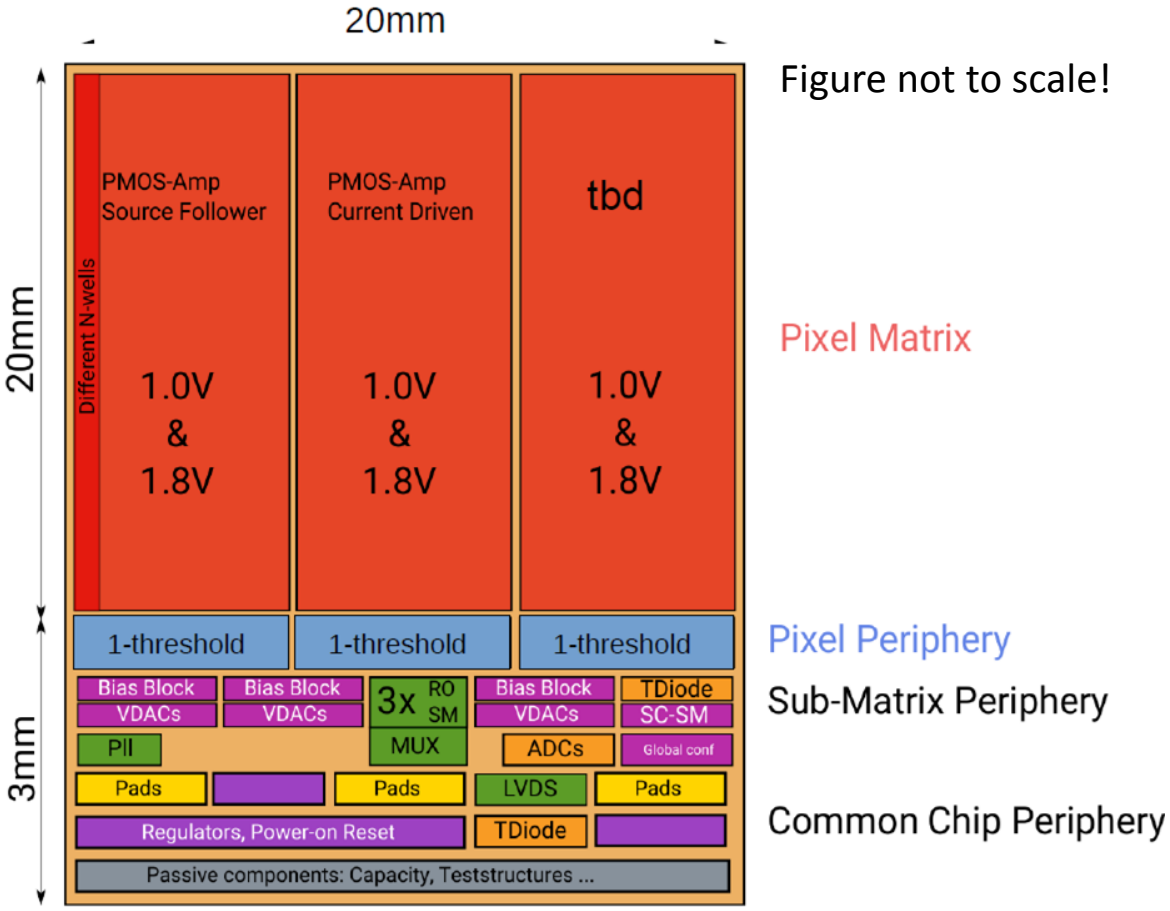
Pixel level

Pixel level with ToT correction (σ = 6.5 ns)

H. Augustin, arXiv:1905.09309v1, 2019

MuPix10 – General design features

- Engineering run in the **180 nm HV-CMOS process from TSI**
- Submitted in December 2019



A. Schoening, VERTEX WS, 2019

ATLAS – Several developments

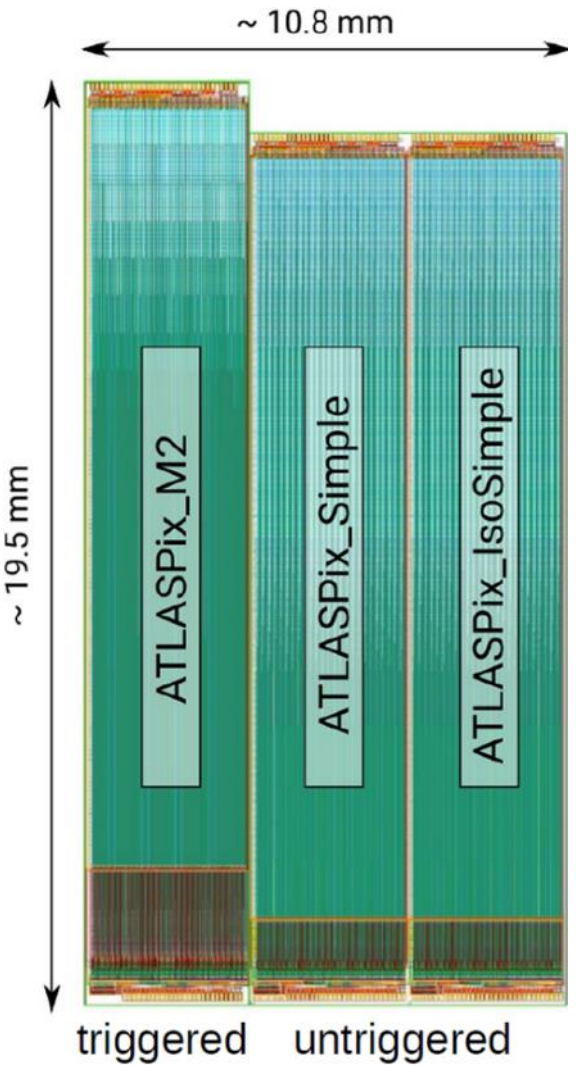
ATLAS – ATLASPix1

ATLASPix1 - General design features

- Engineering run in the **180 nm HV-CMOS process from ams (aH18)**
- Shared with MuPix8 (ATLASPix1 is ~1 cm x 2 cm)

ATLASPix1 – Chip details → 3 sub-matrices

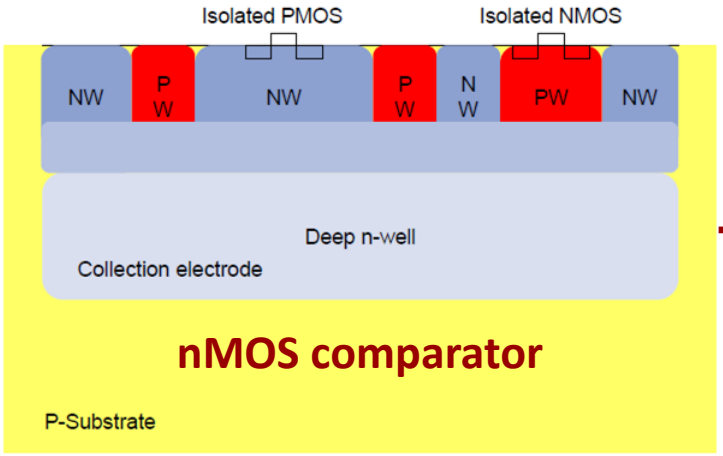
- **ATLASPix_M2:** Triggered readout + no deep p-well
  - Matrix with 56 x 320 pixels
  - 60 µm x 50 µm pixel size
  - Trigger buffers (latency < 25 µs)
- **ATLASPix_Simple:** Continuous readout + no deep p-well
  - Matrix with 25 x 400 pixels
  - 130 µm x 40 µm pixel size
  - 300 mW/cm^2
- **ATLASPix_IsoSimple:** Continuous readout + deep p-well
  - Identical to previous matrix, but with deep p-well
- Discriminators in active pixel cell
- 10-bit TS (double check) and 6-bit ToT
- State machine
- Serial link < 1.6 Gbit/s



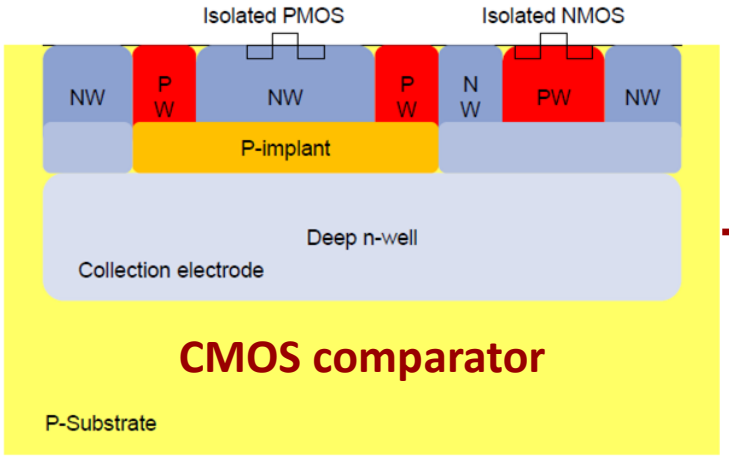
A. Schoening, VERTEX WS, 2018

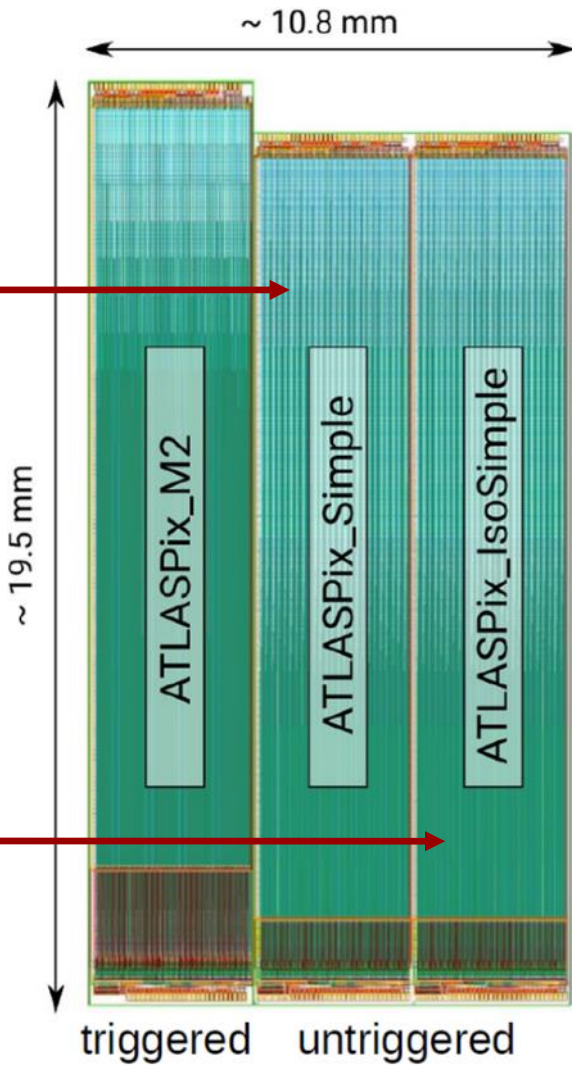
ATLAS – ATLASPix1

Traditional cross-section



New cross-section



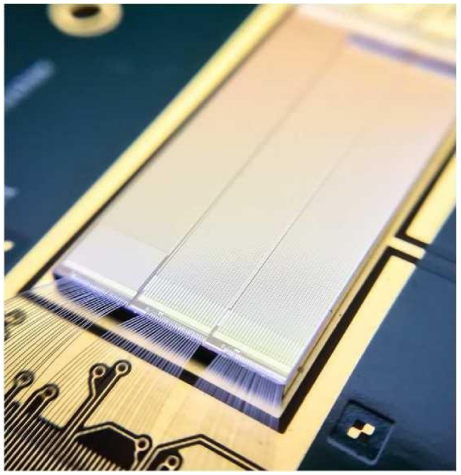


I. Peric, TREDI WS, 2017

A. Schoening, VERTEX WS, 2018

ATLASPix1 – Efficiency

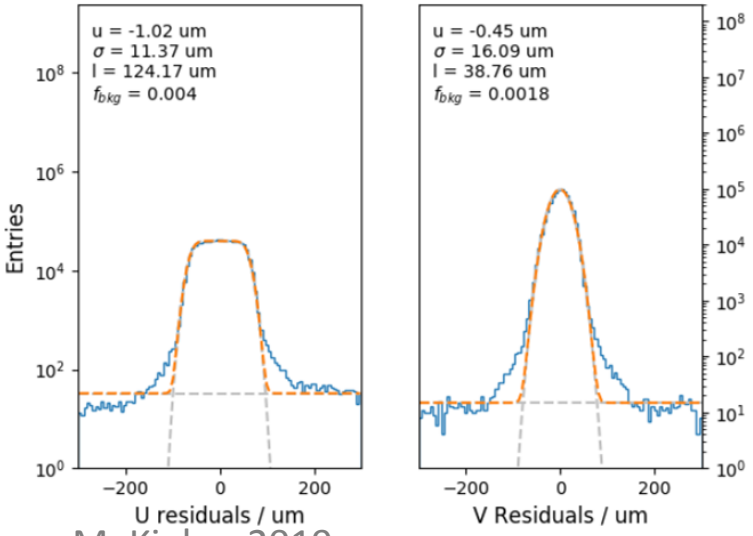
Test beam campaign at Fermilab and CERN (**before**/after irradiation)



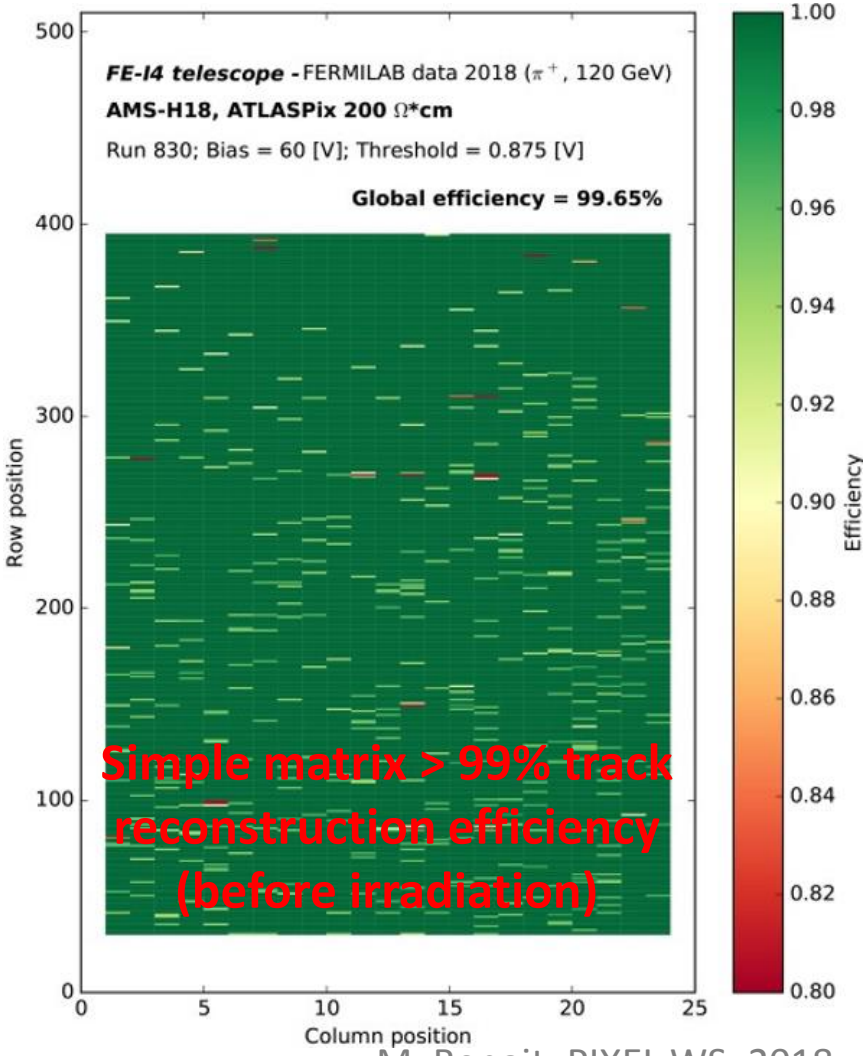
- 200 Ω·cm
- 60 µm thin
- 60 V bias voltage

Residuals

- 60 µm thin
- 65 V bias voltage
- Good alignment



M. Kiehn, 2019

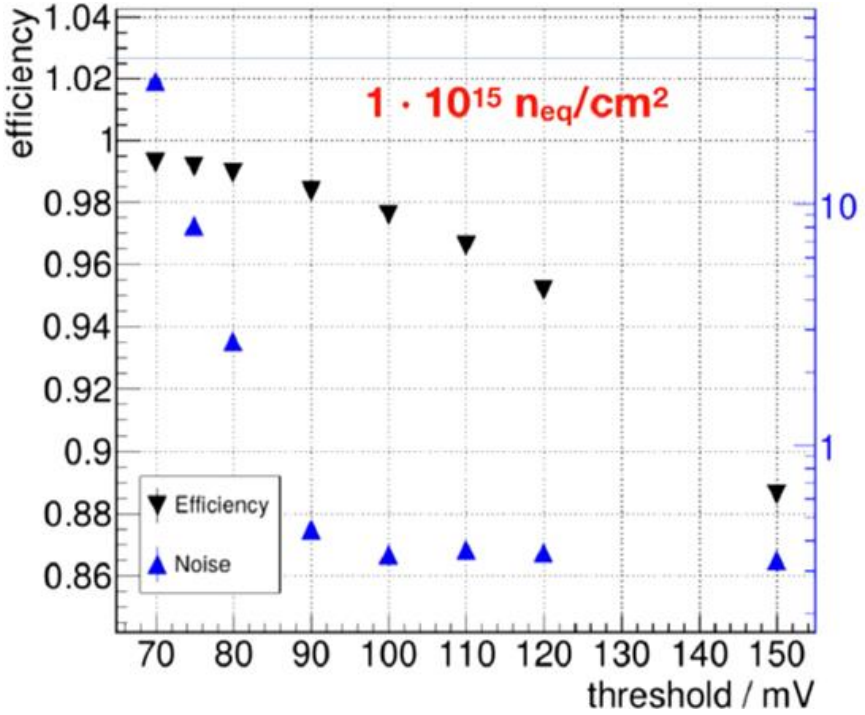


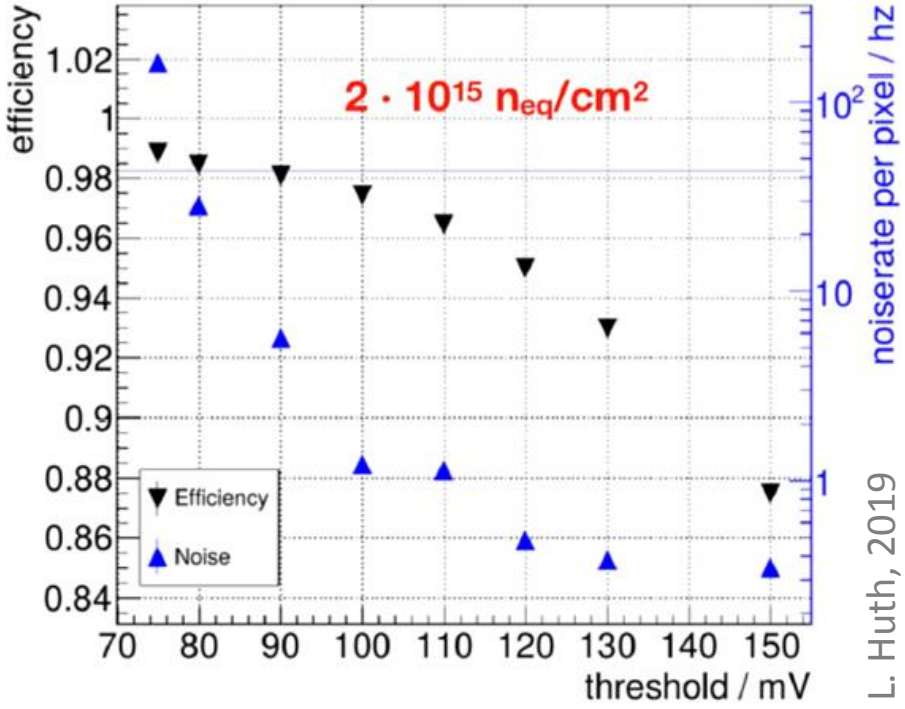
M. Benoit, PIXEL WS, 2018

ATLASPix1 – Efficiency

Test beam campaign at Fermilab and CERN (before/**after** irradiation)

- 80 Ω·cm samples
- 60 µm thin
- 60 V bias voltage
- 10° C temperature





- **Very high efficiency after 10^{15} n_{eq}/cm^2 fluences** (threshold dependent)
- Low noise (dominated by single pixels)

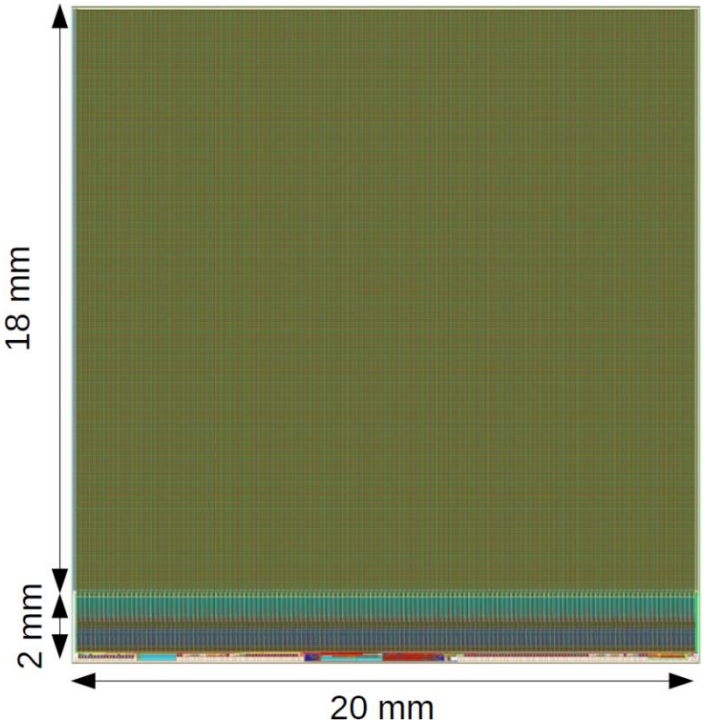
ATLAS – ATLASPix3

ATLASPix3 - General design features

- Engineering run in the **180 nm HV-CMOS process from TSI**
- Total chip area is 2 cm x 2 cm
- Fabricated in 2019

ATLASPix3 – Chip details

- Matrix with 132 columns x 372 rows
- 150 µm x 50 µm pixel size
- In-pixel comparator
- Column drain readout with and without trigger
- Trigger latency < 25 µs
- Radiation hard design with SEU tolerant global memory
- Serial powering (only one power supply needed)
- Data interface is very similar to RD53 readout chip (ATLAS)
- Power consumption is ~200 mW/cm^2 (with 25 ns time resolution)
- Very initial measured results available
- Expected radiation tolerance is 100 Mrad and 1 x 10^{15} 1 MeV n_{eq}/cm^2

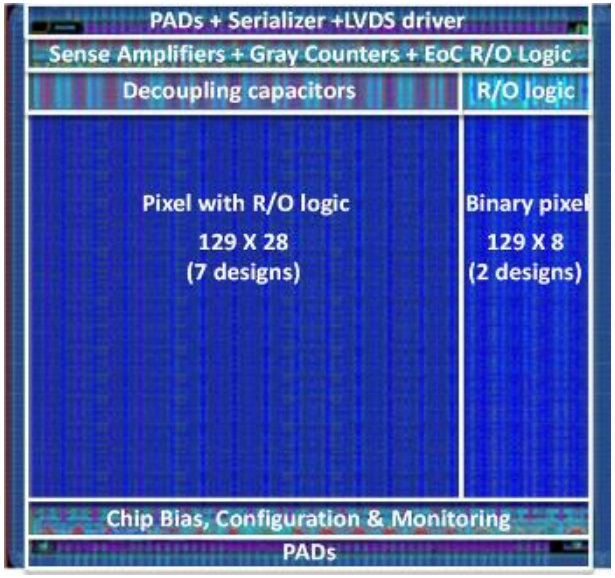


R. Schimassek, Mu3e collaboration meeting, 2019

ATLAS – LF-MonoPix1

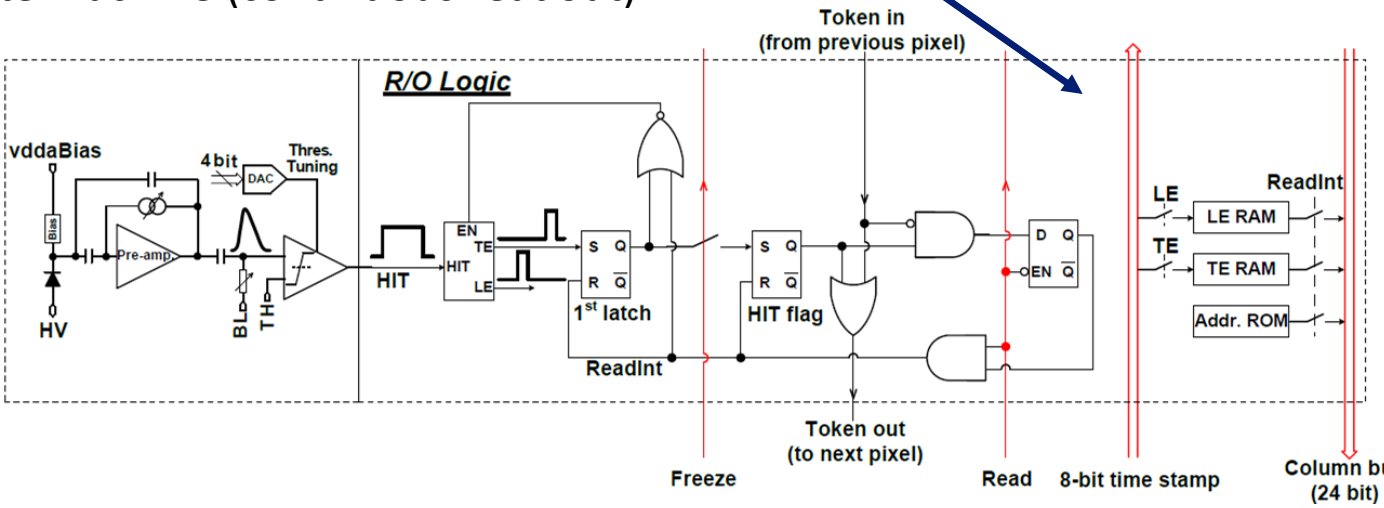
LF-MonoPix1 - General design features

- Large MPW run in the **150 nm HV-CMOS process from LFoundry**
- Total chip area is 10 mm x 9.5 mm
- Fabricated in 2016
- Fabricated using a 2 kΩ·cm substrate resistivity



LF-MonoPix1 – Chip details

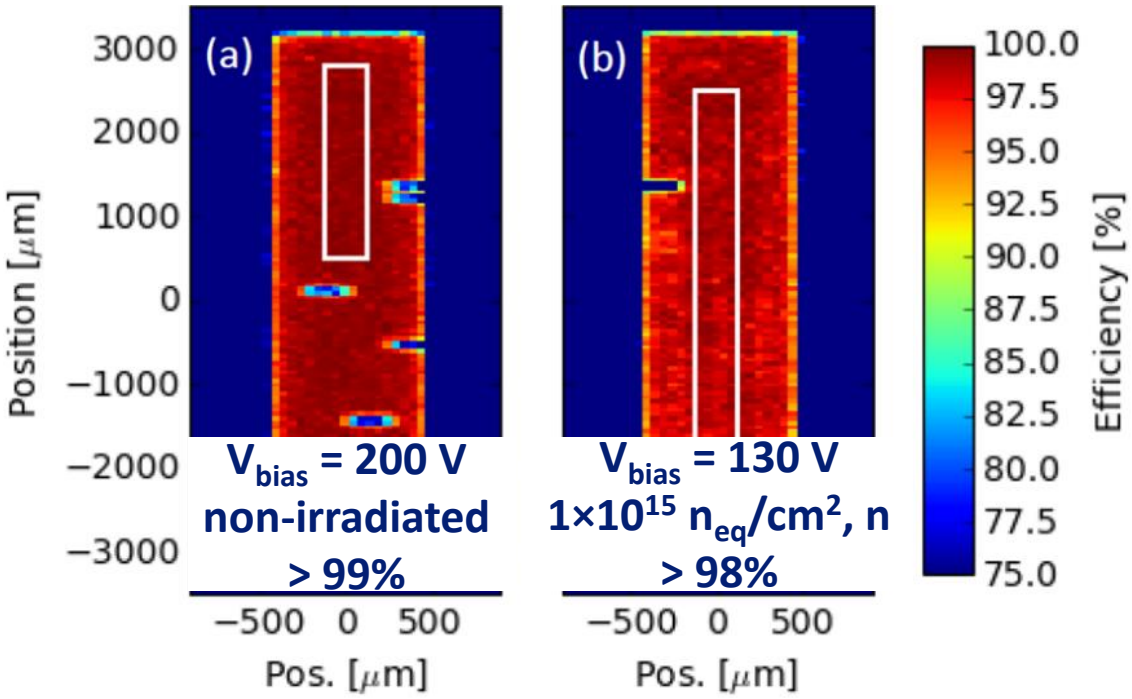
- Matrix with 129 columns x 26 rows
- 50 µm x 250 µm pixel size
- **In-pixel analog and digital readout electronics**
- State machine (continuous readout)



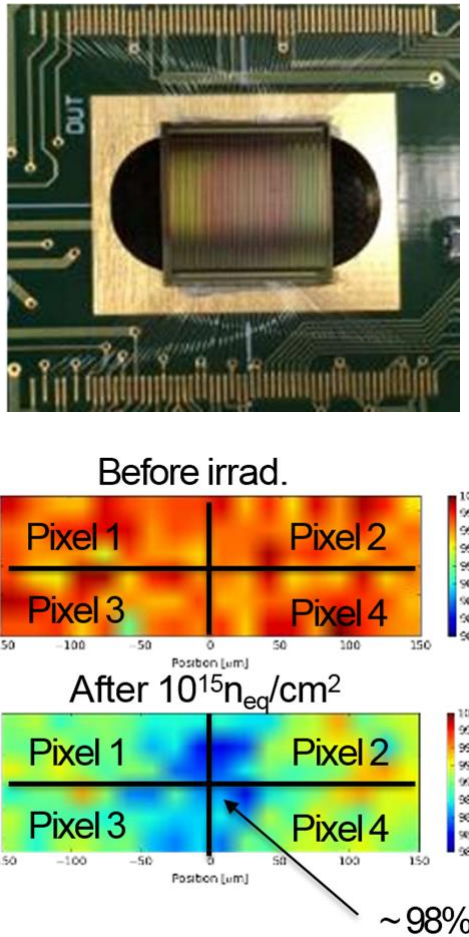
T. Wang, arXiv:1611.01206v1, 2016

ATLAS – LF-MonoPix1

Test beam campaign at ELSA with 2.5 GeV electron beam (before/after irradiation)



T. Hirono, 2018

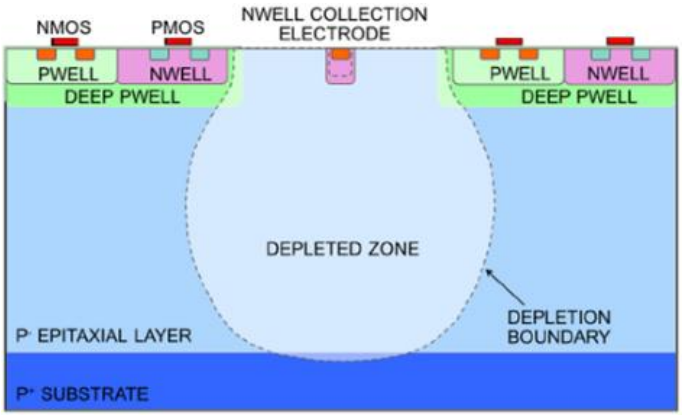


T. Wang, 2018

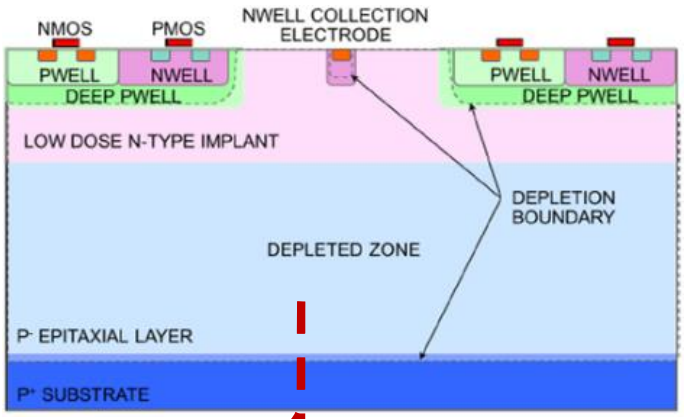
- Most Probable Value (MPV) decreases after 10^{15} n_{eq}/cm^2 fluences, but very high efficiency

ATLAS – Investigator

Standard TowerJazz process



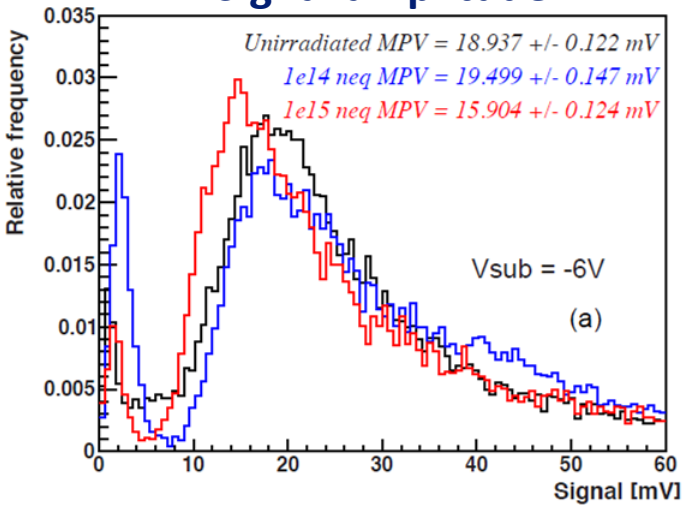
Modified TowerJazz process



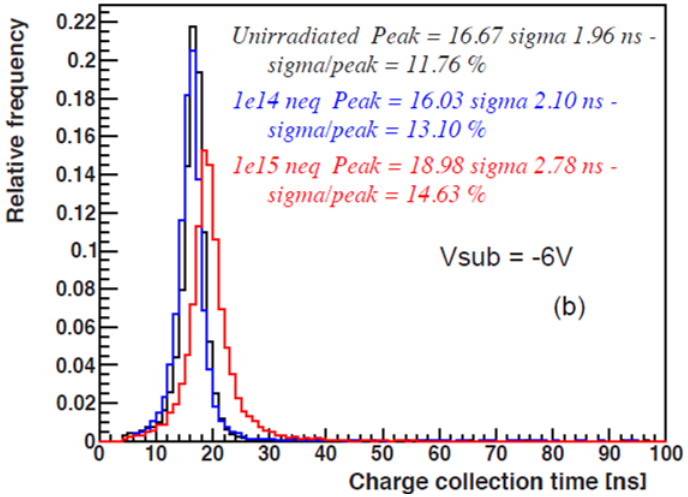
W. Snoeys, 2017

Sr-90 source tests

Signal amplitude



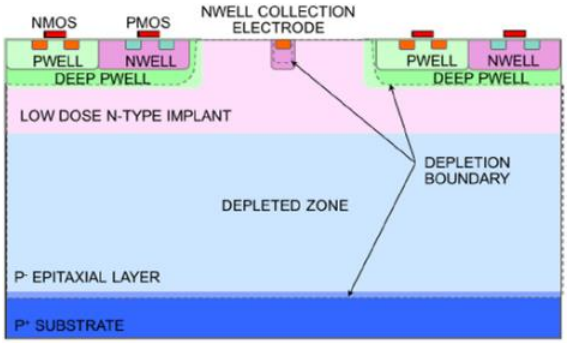
Signal rise time



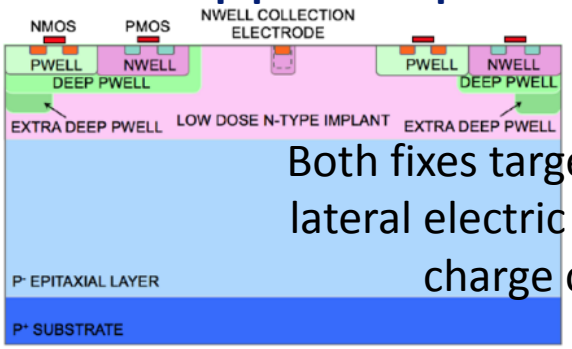
I. Berdalovic, 2018

ATLAS – MiniMALTA

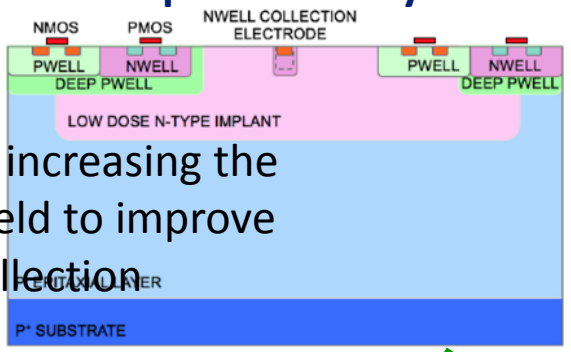
Modified TowerJazz process



Extra deep p-well implant

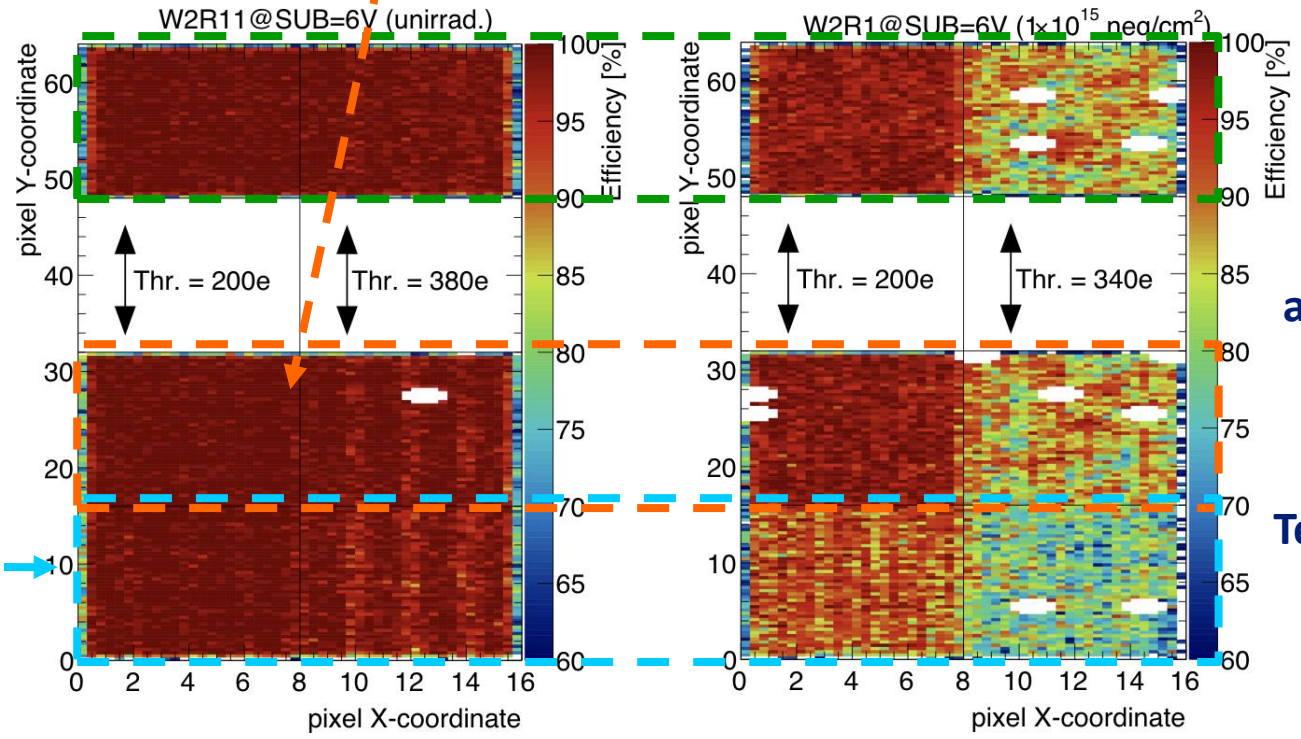


Gap in the n-layer



Both fixes target increasing the lateral electric field to improve charge collection

B. Hiti, 2018

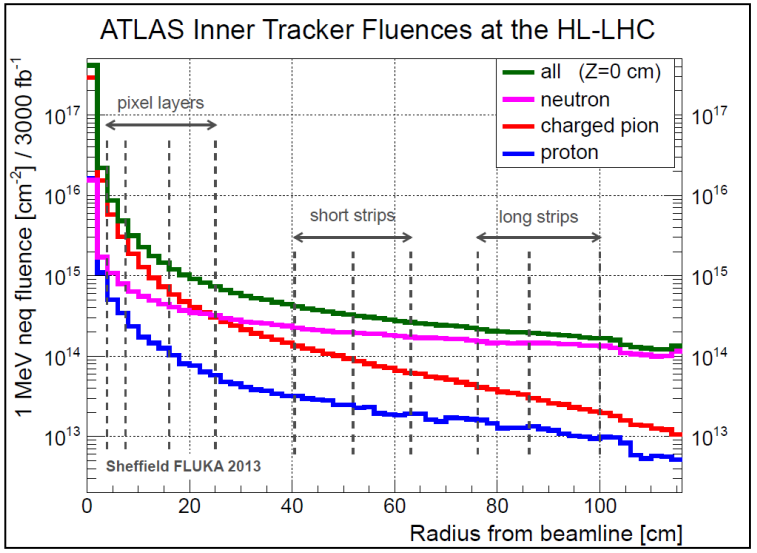


98-99% efficiency after 1×10^{15} n_{eq}/cm^2

Test beam at DESY and ELSA

CERN-RD50

- An **international R&D collaboration** aimed at developing radiation hard semiconductor devices for high luminosity colliders:
  - High Luminosity-LHC (HL-LHC)
    ➔ > 10^{16} 1 MeV n_{eq}/cm^2
  - Future Circular Collider (FCC)
    ➔ > 7×10^{17} 1 MeV n_{eq}/cm^2
- Detectors used now at LHC cannot operate after such irradiation. CERN-RD50 is studying new structures:
  - N in p sensors
  - 3D
  - LGAD
  - DMAPS



I. Dawson, ATL-UPGRADEPUB-2014-003, 2014

- **CERN-RD50 work package to develop and study DMAPS with high priority:**
  - ASIC design, TCAD simulations, DAQ development and performance evaluation
  - ~25 people from ~12 institutions

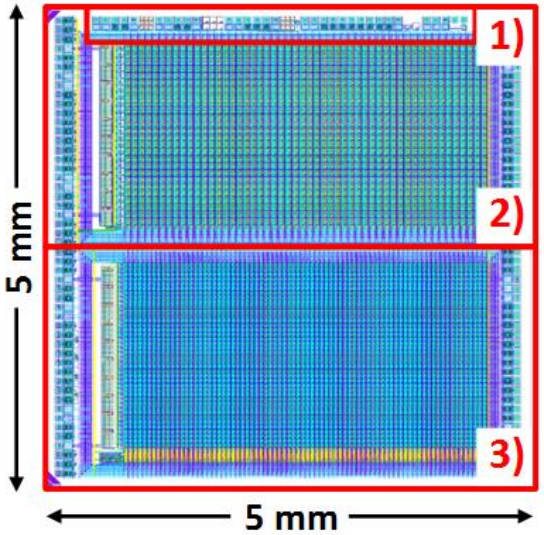
CERN-RD50 – RD50-MPW1

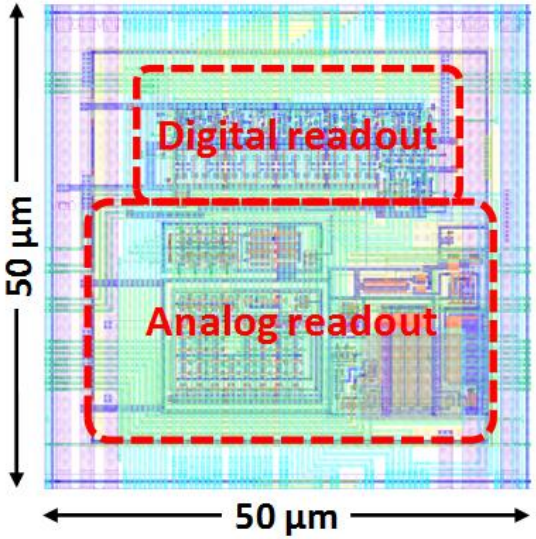
RD50-MPW1 - General design features

- MPW in the **150 nm HV-CMOS process from LFoundry**
- Submitted in November 2017, received in April 2018
- To gain expertise and develop new designs
- Fabricated using 2 different substrate resistivities
  - 600 Ω·cm and 1.1 kΩ·cm

RD50-MPW1 – Chip details

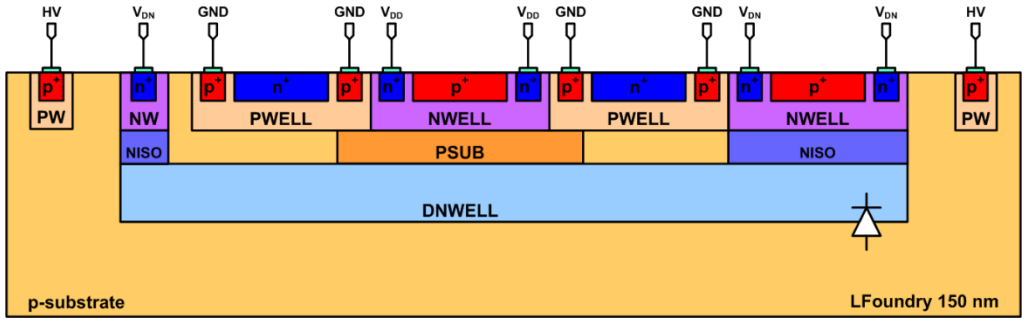
1) Test structures for eTCT measurements
2) Matrix of DMAPS pixels with 16-bit counter
   - 26 rows x 52 columns
   - 75 µm x 75 µm pixel size
   - Aimed at photon counting applications (proof-of-concept)
3) **Matrix of DMAPS pixels with continuous readout (FE-I3)**
   - 40 rows x 78 columns
   - 50 µm x 50 µm pixel size
   - Aimed at particle physics applications
- Analog and digital readout embedded in the sensing area of the pixel



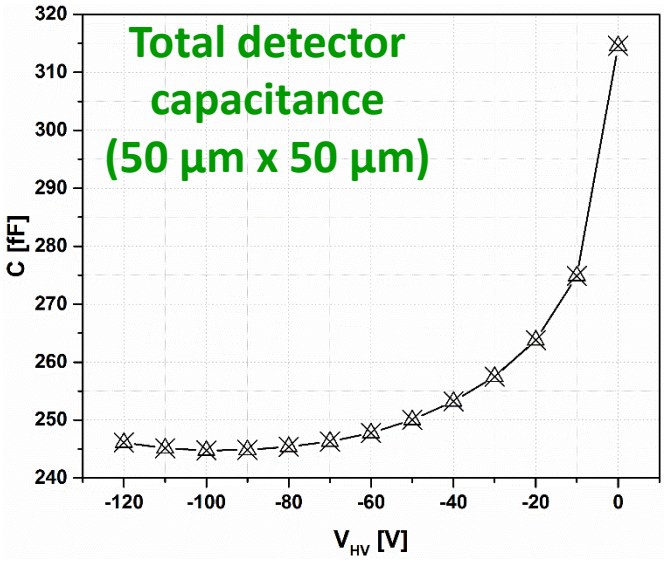


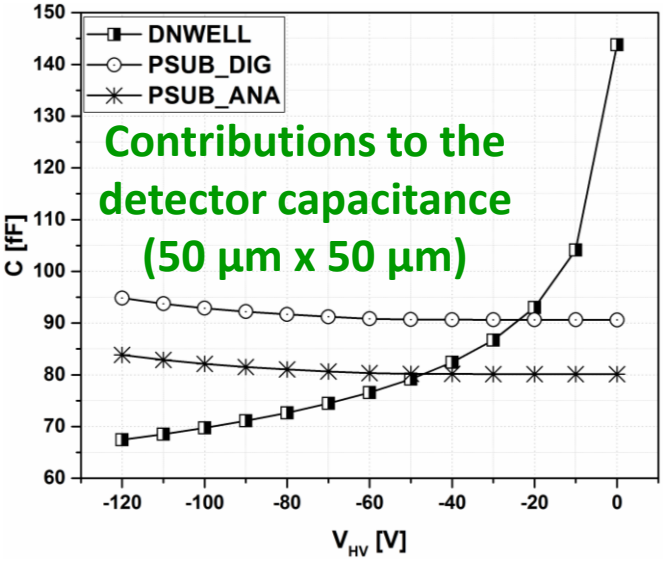
RD50-MPW1 – Sensor

Sensor cross-section

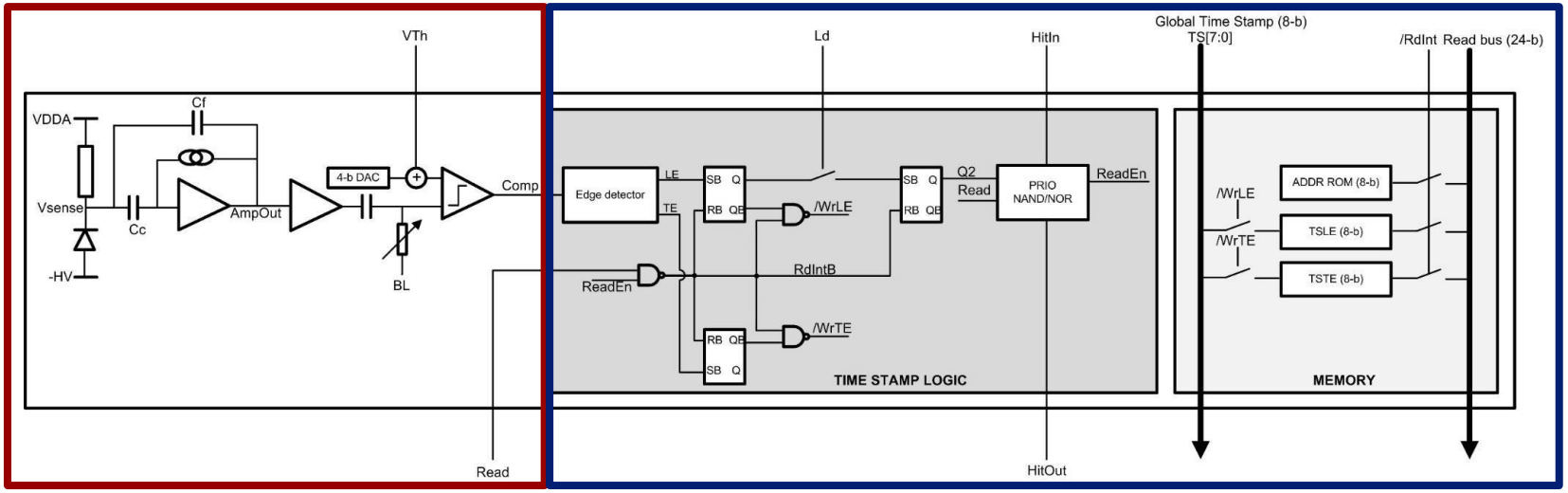


- Large fill-factor pixel
- PSUB layer isolates NWELL from DNWELL
  - CMOS electronics in pixel area are possible
- Detector capacitance has 2 contributions
  - P-substrate/DNWELL
  - PSUB/DNWELL
- Total pixel capacitance (50 µm x 50 µm) ~250 fF
- Equivalent Noise Charge (ENC) ~100 – 120 e^-





RD50-MPW1 – Readout electronics



Analog readout

- Sensor biasing circuit, CSA, RC-CR filters and CMOS comparator
- CSA with programmable discharging current
- CMOS comparator with global VTH and local 4-bit DAC for fine tuning

Digital readout

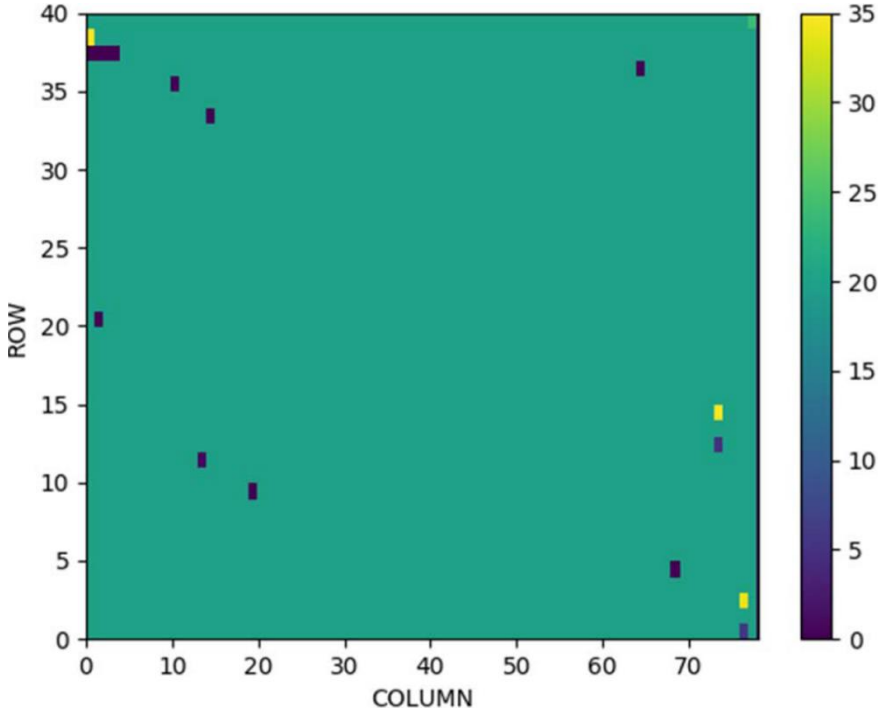
- Continuous readout (synchronous, triggerless, hit flag + priority encoding)
- Global 8-bit Gray encoded time-stamp (40 MHz)
- For each hit
  - ➔ Leading edge (LE): 8-bit DRAM memory
  - ➔ Trailing edge (TE): 8-bit DRAM memory
  - ➔ Address (ADDR): 6-bit ROM memory

  } ➔ TOT = LE – TE (off-chip)

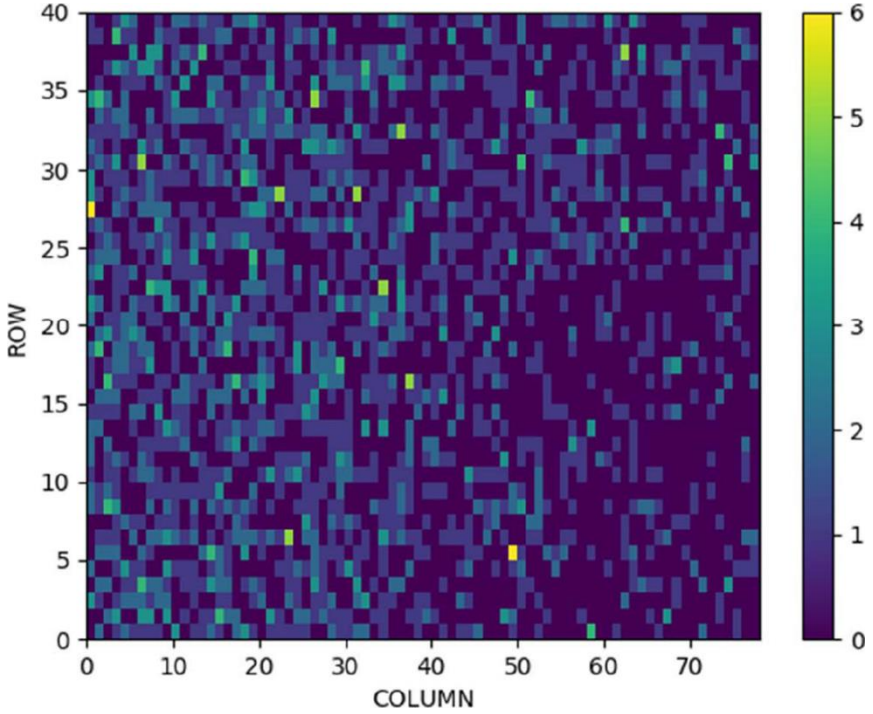
RD50-MPW1 – Measured results

Hit maps

- Calibration circuit
  - 1 MHz readout speed
  - 20 test pulses per pixel
  - 1.5 V test pulses

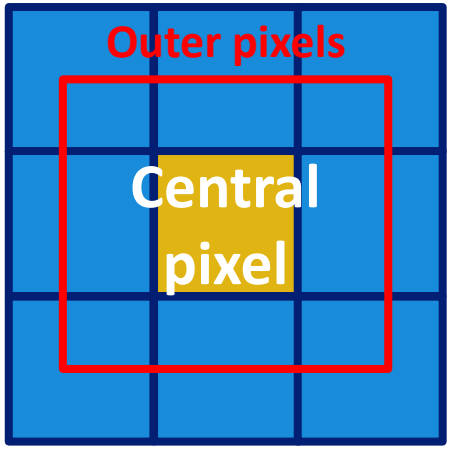


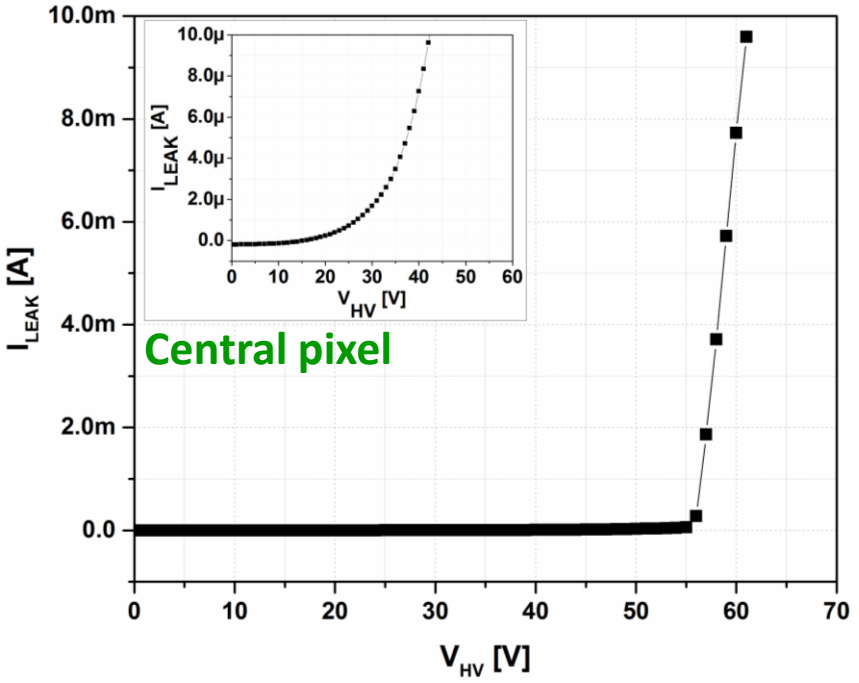
- Radioactive source
  - 1 MHz readout speed



H. Steininger, internal meeting, 2019

RD50-MPW1 – Measured results

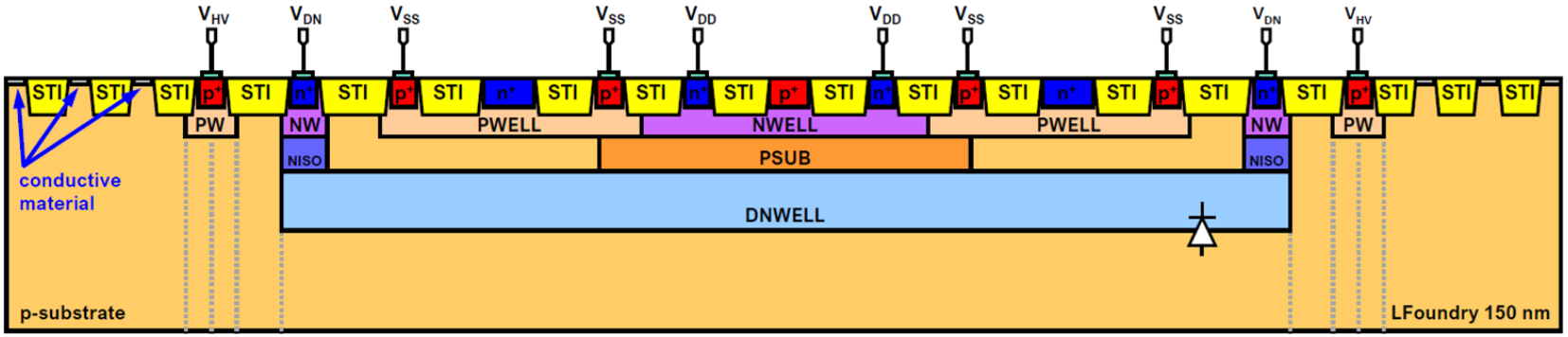




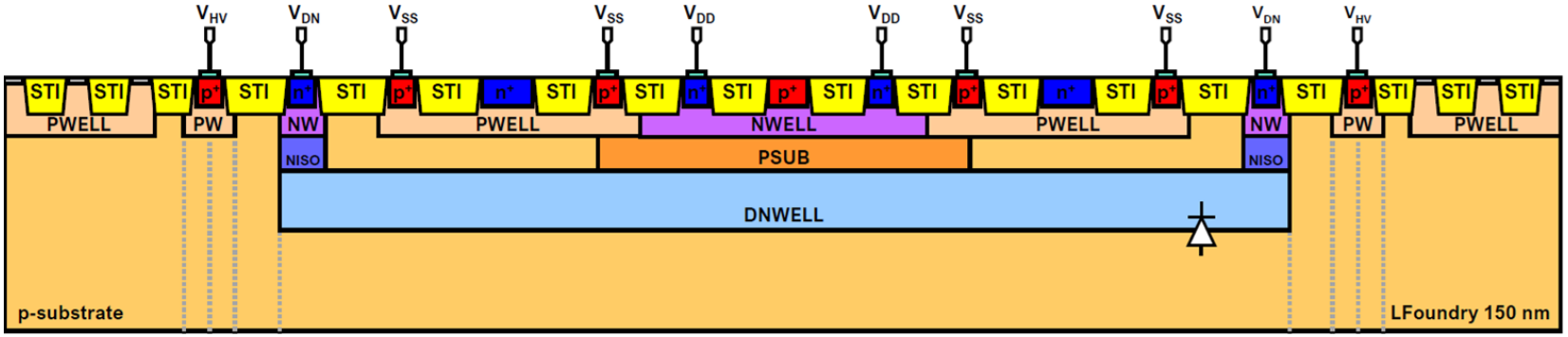
I-V curve

- I-V of central pixel of test structure (pixel size is 50 µm x 50 µm)
- Measurement done using a probe station with sensor in complete darkness
- **VBD ~ 55-60 V as expected from the design**
- **ILEAK is too high (µA order well before VBD)**
- This issue has been extensively studied: *TCAD* + *support from the foundry*
- Methodologies to optimize leakage current in *new prototype RD50-MPW2*

Post-processing – Lessons learned



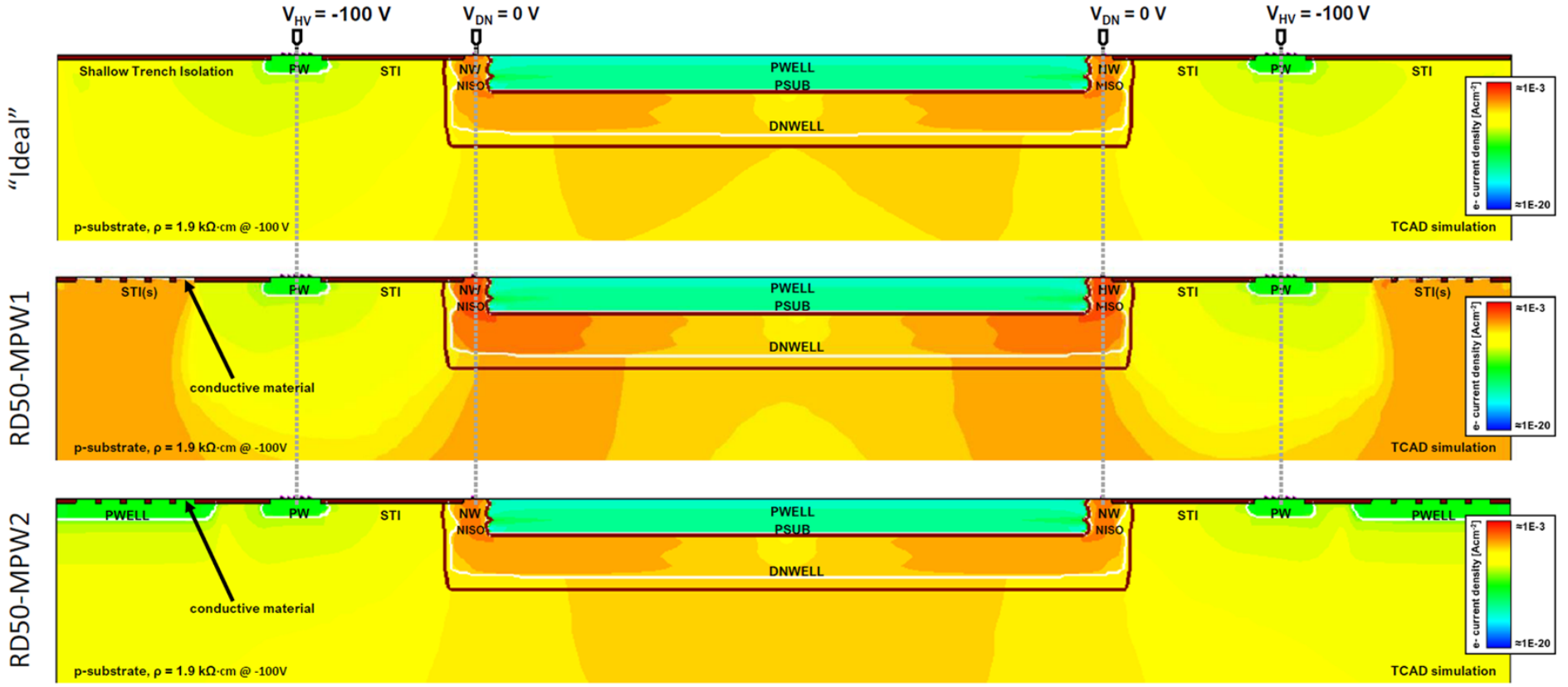
- LFoundry adds structures to the design files to prepare them for fabrication.
- These structures **involve conductive material**.
- We believe these structures **contribute quite significantly to the high ILEAK**.



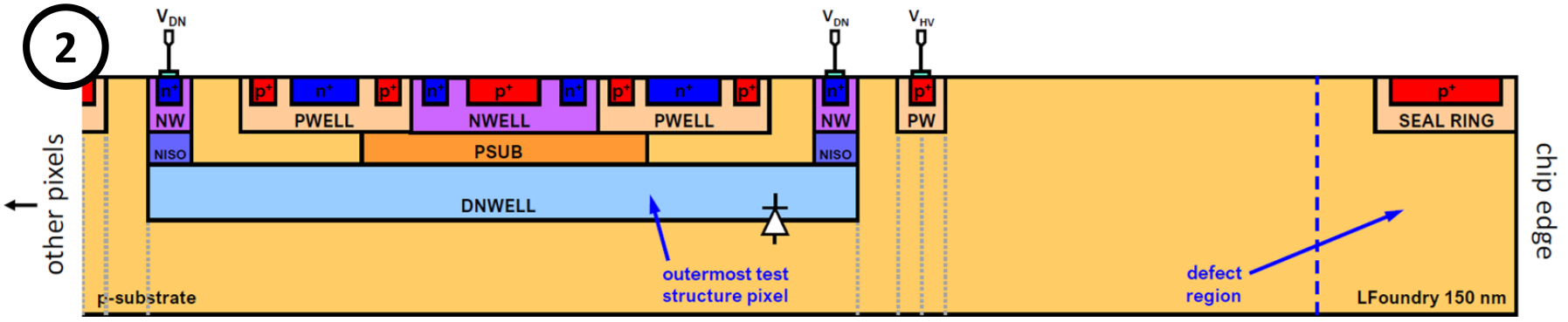
- We have **minimised the presence of these structures** as much as possible.
- Wherever not possible, LFoundry suggested **placing these structures inside a PWELL**.

Post-processing – TCAD simulations

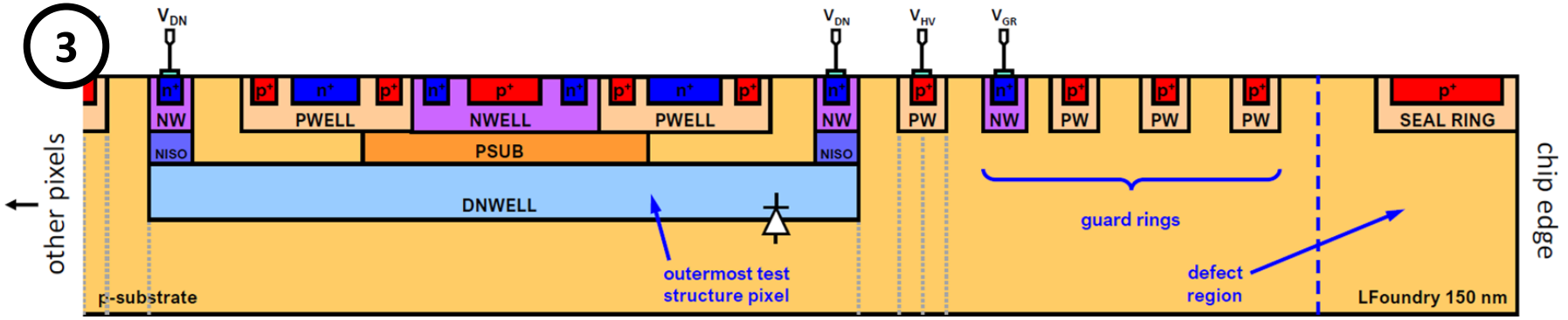
Electron-current density



Edge defects – Lessons learned

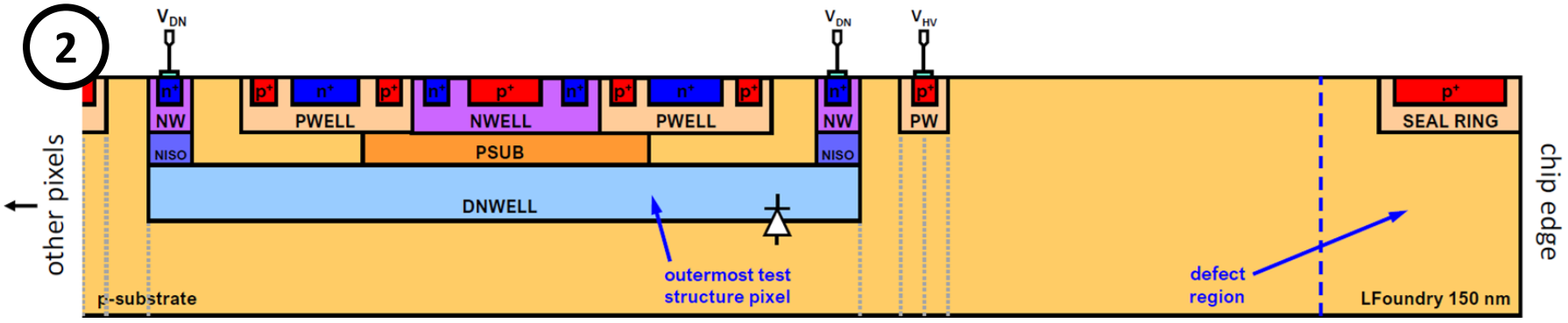


- Some pixels can be quite close to the edge of the chip
- Defects in silicon lattice due to dicing can become significant
- ILEAK increases when the pixel depletion region is near the defect region



- **N-type guard ring** added as safeguard to "collect" leakage current
- **P-type guard rings** added to reduce "lateral" depletion

Edge defects – Lessons learned



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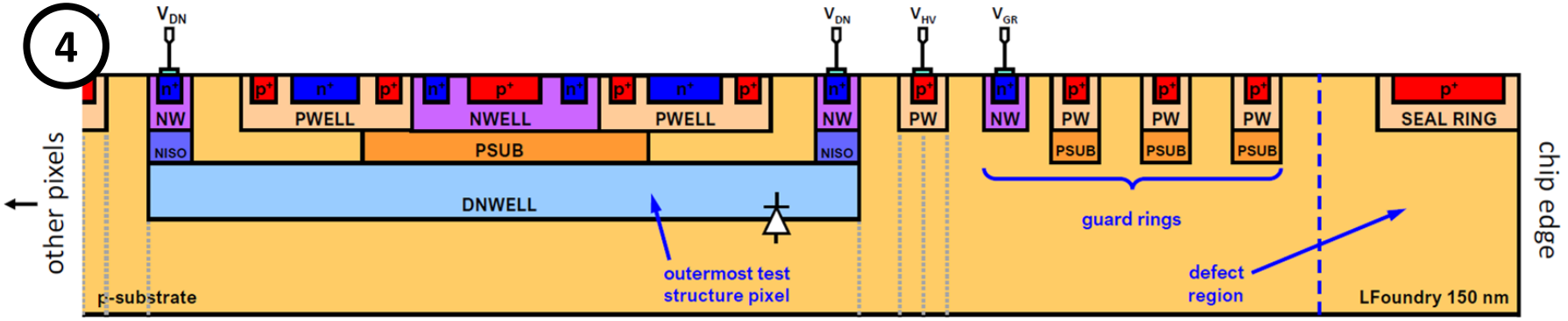
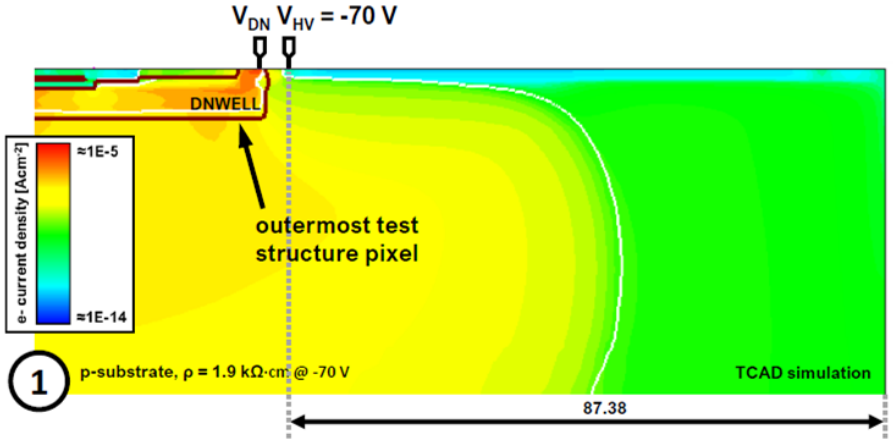
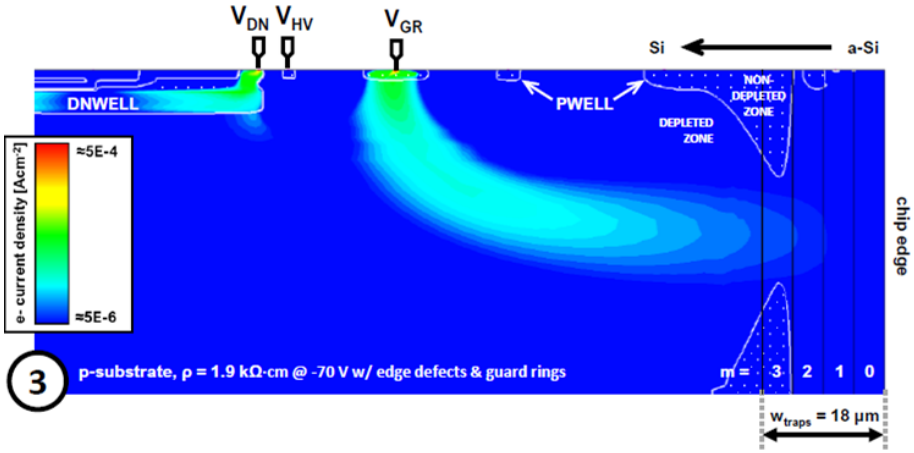
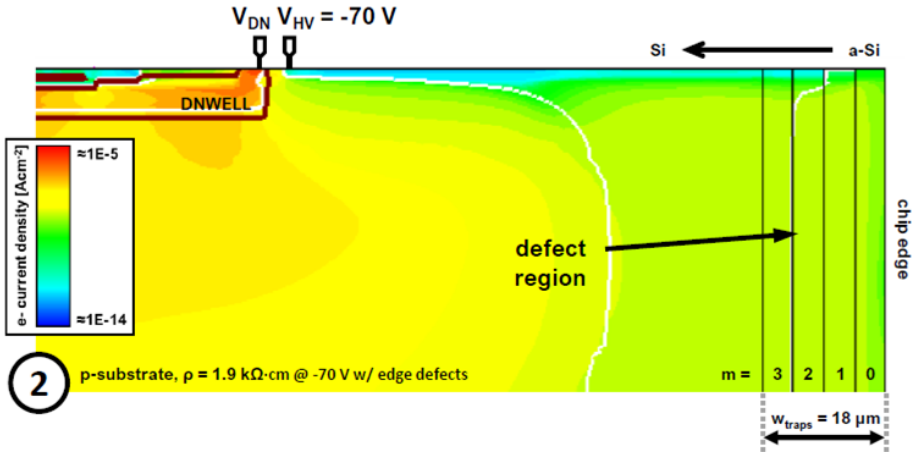


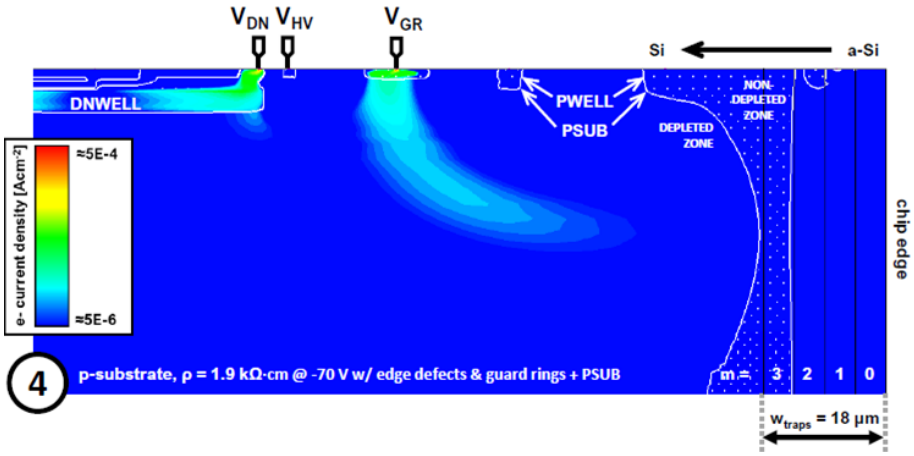
- **N-type guard ring** added as safeguard to "collect" leakage current
- **P-type + PSUB guard rings** added to further reduce "lateral" depletion

Edge defects – TCAD simulations









M. Franks, TREDI WS, 2019

1) Without defects (ideal case)
2) With defects and no guard rings
3) With defects, and NWELL and PWELL guard rings
4) With defects, and NWELL and PWELL with PSUB guard rings

CERN-RD50 – RD50-MPW2

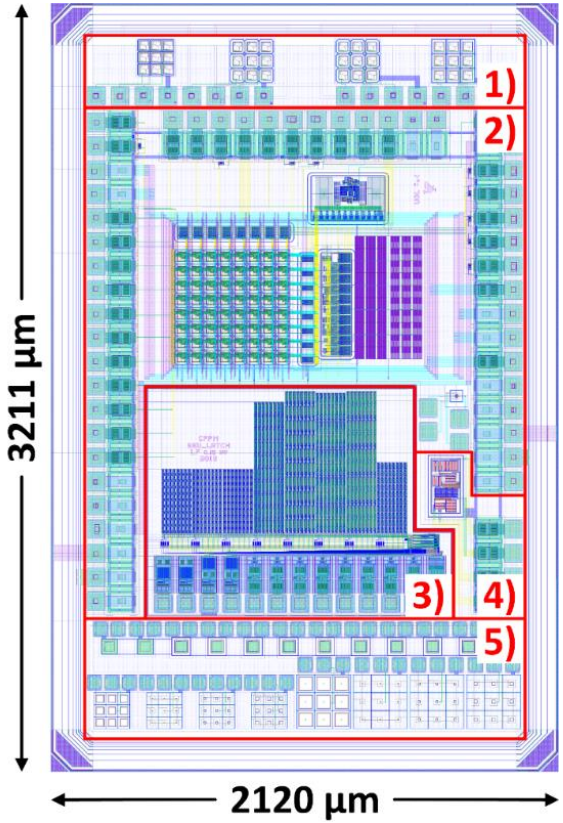
RD50-MPW2 - General design features

- MPW in the **150 nm HV-CMOS process from LFoundry**
- Submitted in January 2019 (dies expected in January 2020)
- To test methods to minimize the leakage current
- Fabricated using 4 different substrate resistivities
  - 10 Ω·cm, 100 Ω·cm, 1.9 kΩ·cm and 3 kΩ·cm

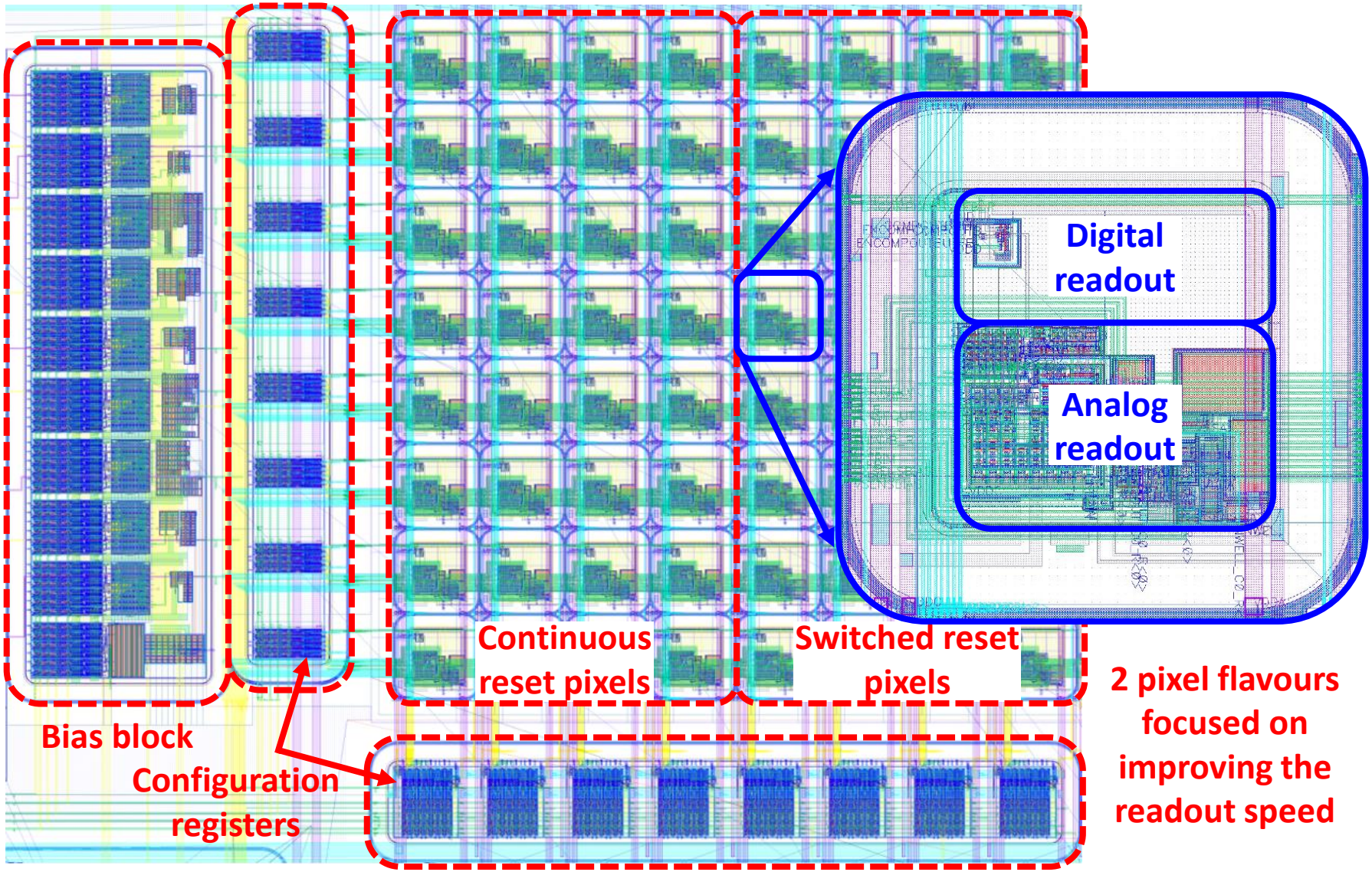
RD50-MPW2 – Chip details

1) Test structures for eTCT measurements
2) Matrix of DMAPS pixels with analog readout only
   - 8 rows x 8 columns
   - 60 µm x 60 µm pixel size
   - Aimed at improving the amplifier response rate
3) SEU tolerant memory array
4) Bandgap reference voltage
5) Test structures with SPADs and DMAPS pixels

- New methodologies to minimize the leakage current



CERN-RD50 – RD50-MPW2



2 pixel flavours focused on improving the readout speed

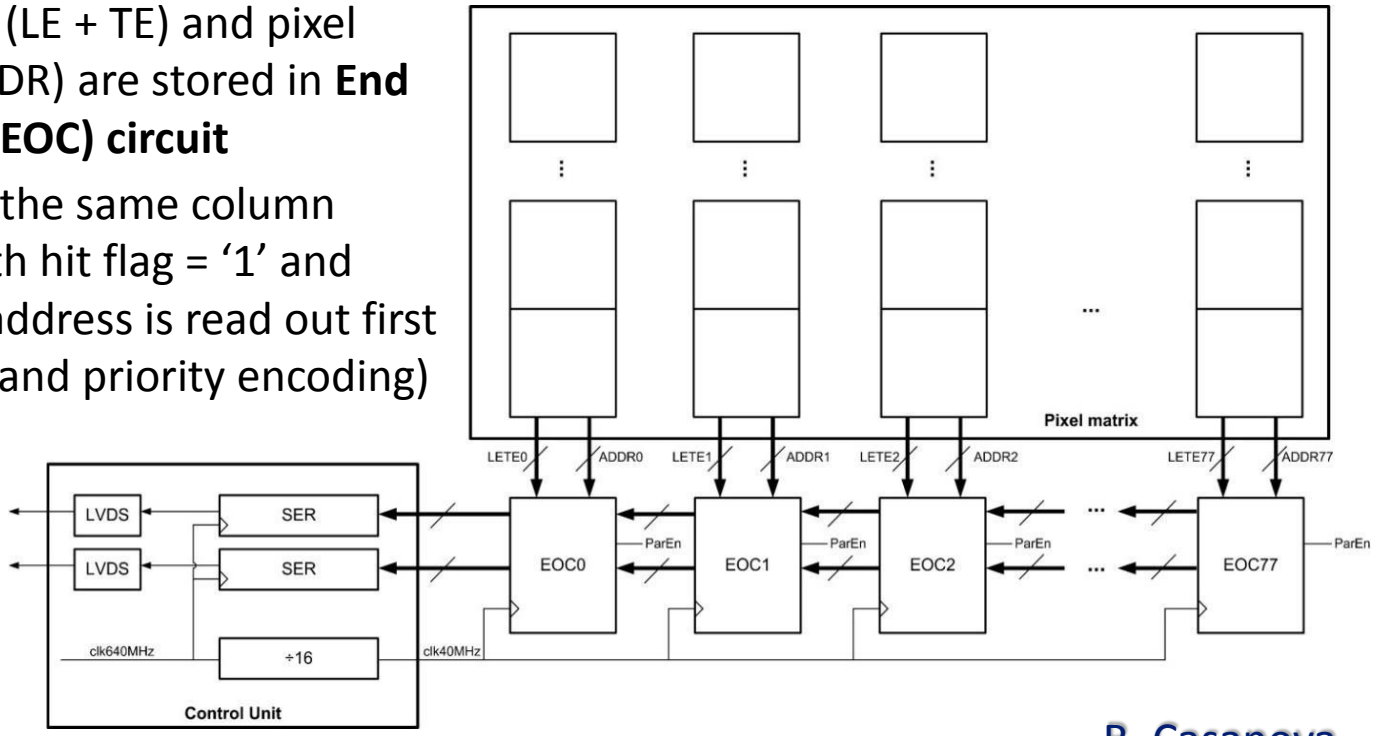
Conclusion

- **DMAPS in HR/HV-CMOS processes have huge potential for future particle physics experiments**
  - Reduced material thickness (50 µm)
  - Small pixel size (50 µm x 50 µm)
  - More cost effective (~£100k/m^2)
  - Fast charge collection by drift (15 ns time resolution)
  - Good radiation tolerance (10^{15} 1MeV n_{eq}/cm^2)
- **Quite a few experiments are interested in DMAPS**
  - Mu3e (first application of DMAPS)
  - ATLAS ITk upgrade (cancelled)
  - LHCb Mighty Tracker upgrade
  - CLIC
  - CERN-RD50 (detector R&D)
- **Several prototypes and "pre-production" detectors developed for these experiments**
- **Detector R&D to further develop its performance done within CERN-RD50**

Back up slides

RD50-MPW1 – Readout architecture

- Time-stamp (LE + TE) and pixel address (ADDR) are stored in **End Of Column (EOC) circuit**
- If > 1 hits in the same column
  - ➔ Pixel with hit flag = '1' and largest address is read out first (hit flag and priority encoding)



R. Casanova, TWEPP 2019

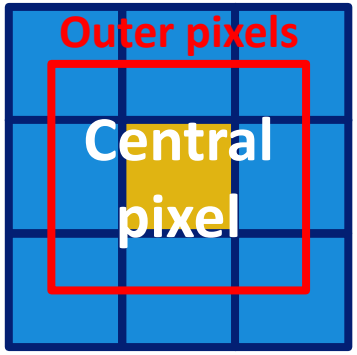
- Shift register with 78 EOC circuits (one EOC per column) @ 40 MHz
- **<u>Continuous readout sequence</u>:**
  1) LE, TE and ADDR of the hit pixel with hit flag = '1' and highest priority stored in EOC (1 clock cycle)
  2) CU reads sequentially the data stored in each EOC @ 40 MHz (78 clock cycles)
  3) Serializers send data off-chip @ max. speed of 640 MHz

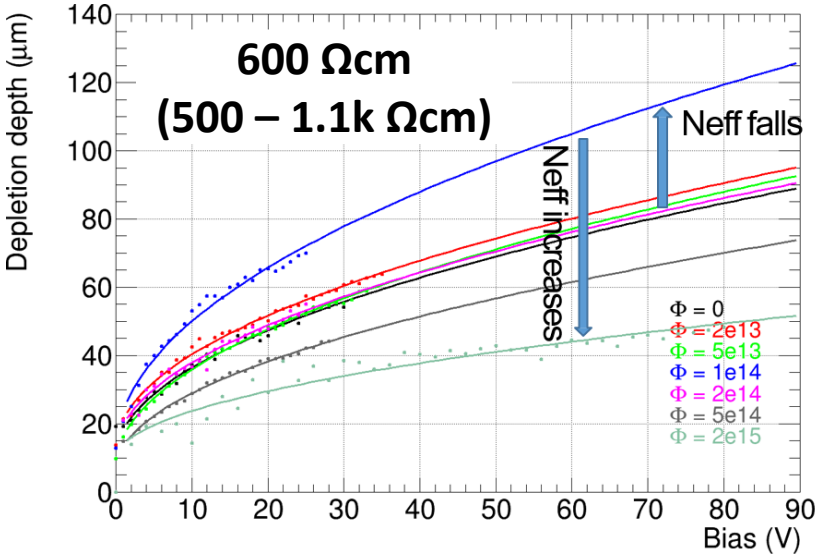
RD50-MPW1 – Measured results

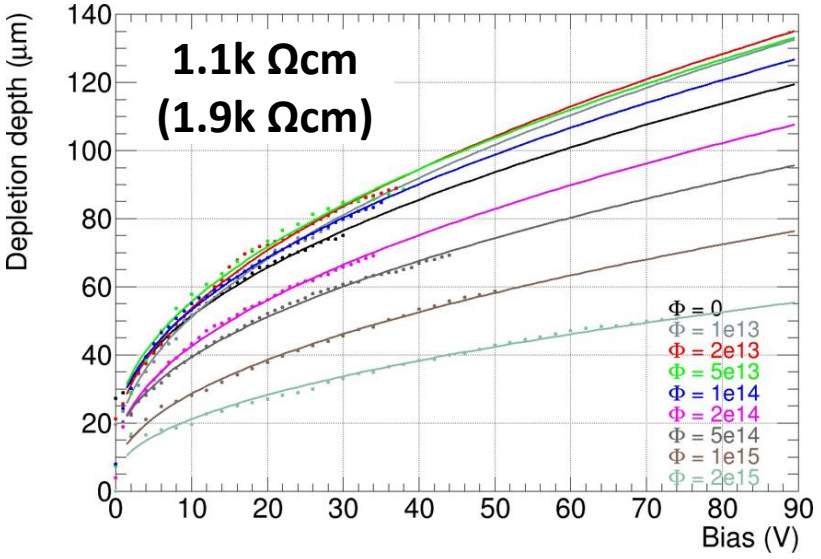
eTCT measurements to study sensor depletion region

I. Mandic, TREDI 2019

- Samples irradiated at TRIGA reactor in Ljubljana to several different n-fluences ranging from 1E13 to 2E15 n_{eq}/cm^2
- **Test structure**
  - ➔ 3 x 3 pixels matrix without readout electronics
  - ➔ Central pixel to read out
  - ➔ Outer pixels connected together
  - ➔ Pixel size is 50 µm x 50 µm

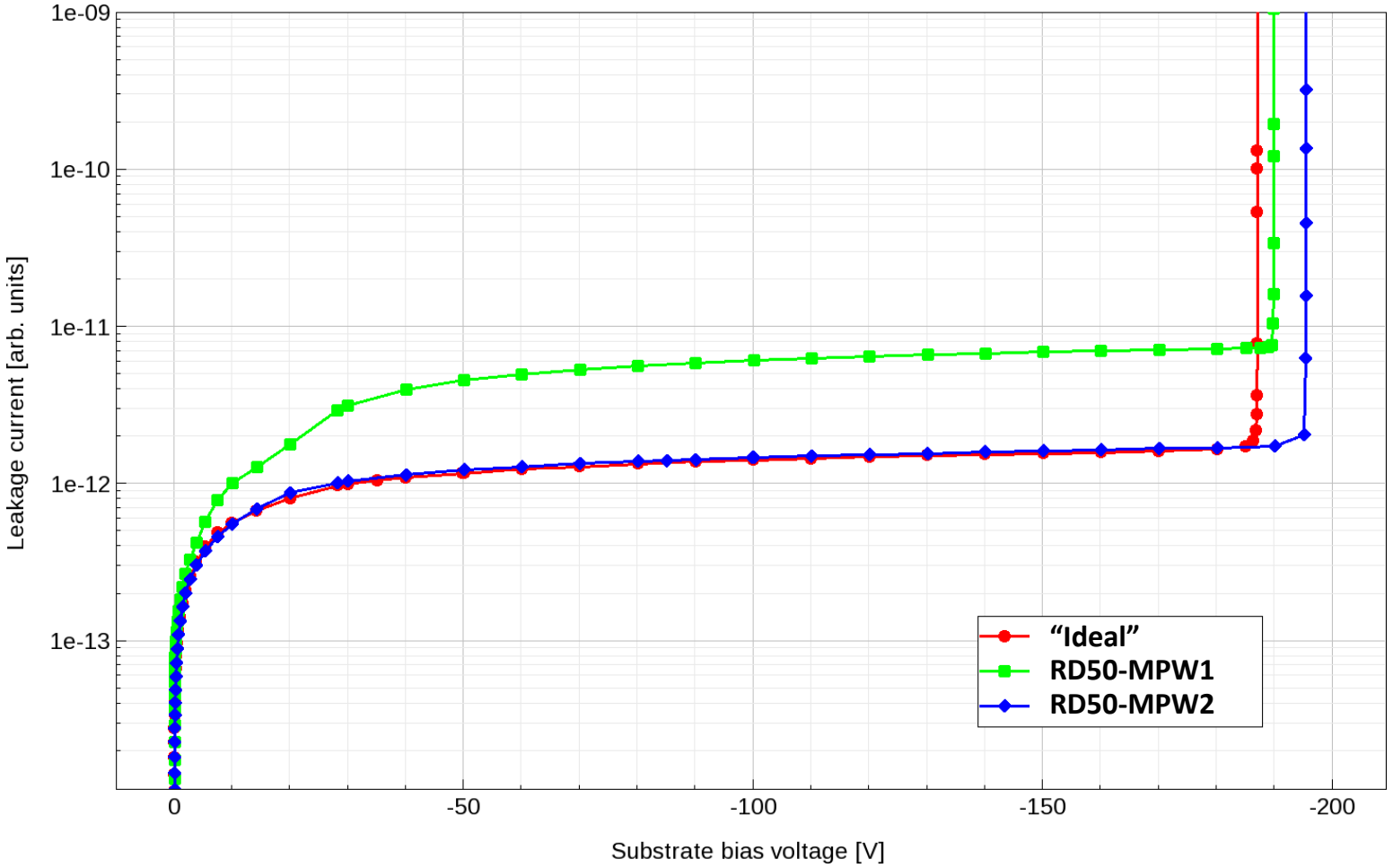






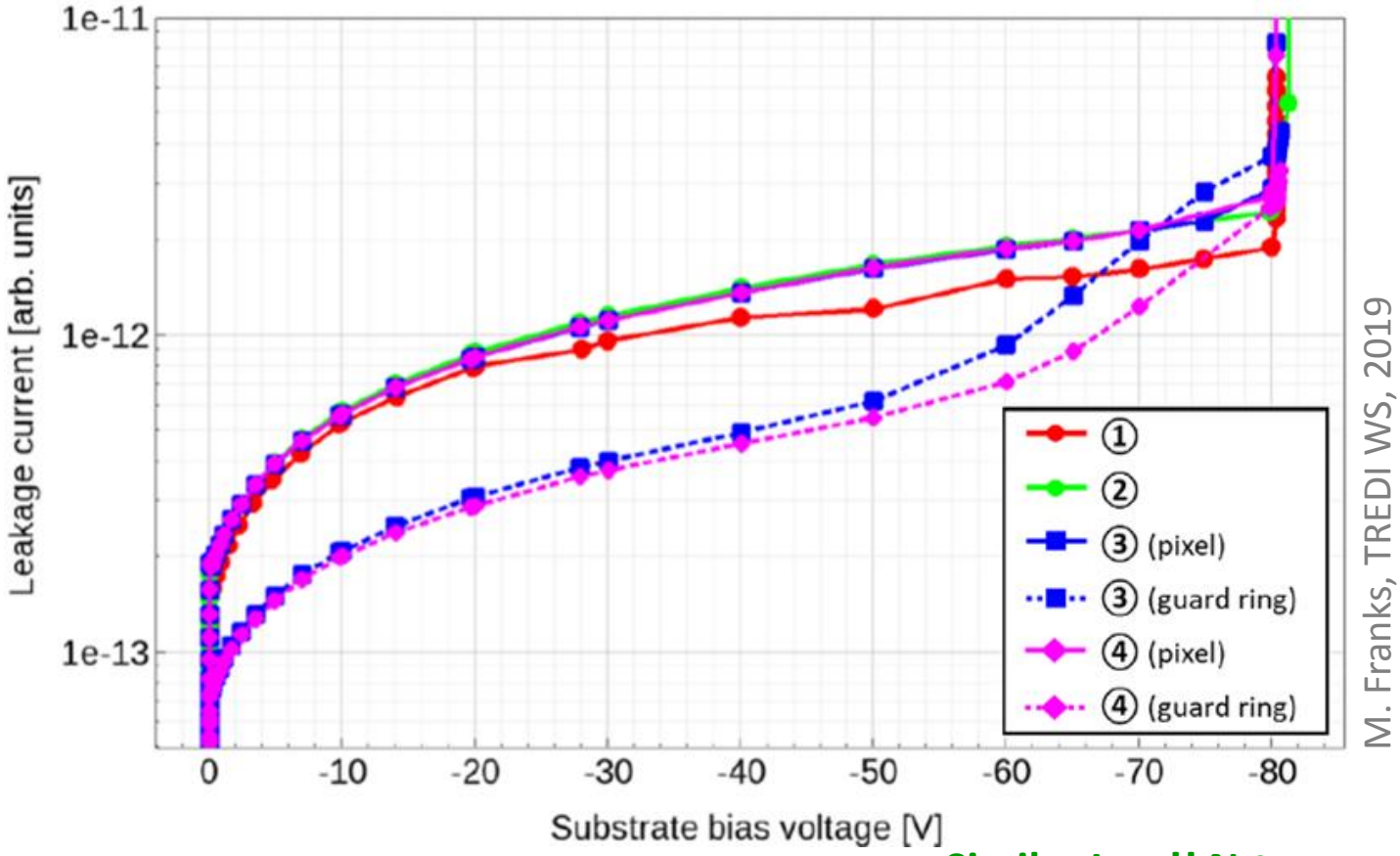
- Depletion depth changes with irradiation + acceptor removal effects seen

TCAD simulations – Post-processing



- Increase in ILEAK when conductive material is present on the surface (RD50-MPW1).
- ILEAK is reduced when conductive material is placed in PWELL (RD50-MPW2).

TCAD simulations – Edge defects



M. Franks, TREDI WS, 2019

1) Without defects (ideal case)
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Similar I_{LEAK}!! N-type guard ring acts as a diode increasing lateral depletion into defect region. PSUB reduces I_{LEAK} ☺

TCAD simulations – Pixel geometry

3D simulations – Electric field as a function of corner geometry in pixel