UNIVERSITY OF BIRMINGHAM

Novel silicon detector technologies for the HL-LHC and beyond

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Particle Physics Seminar, Uni Birmingham

24 November 2021

Outline

- Introduction to silicon detectors with examples from state-of-the-art technology
- Challenges for future tracking detectors and R&D roadmap
- Timing detectors
- CMOS sensors
- Conclusion

Segmented silicon detectors

- Highly segmented silicon detectors are the technology of choice for vertex and tracking detectors at collider experiments

- They detect the passage of ionizing radiation with good spatial resolution and efficiency in the harsh experimental conditions close to the interaction point

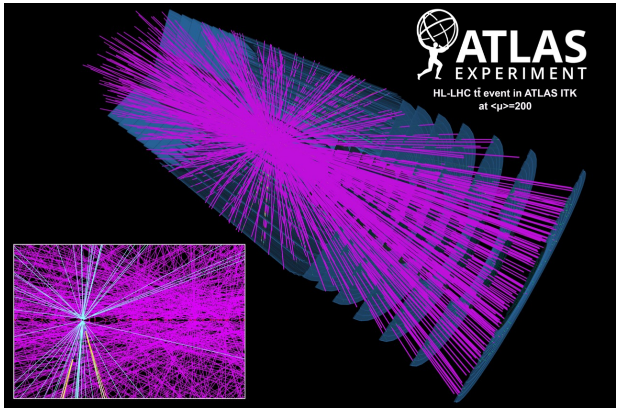
- Different types of silicon detectors exists to satisfy a range of requirements in terms of spatial resolution, radiation hardness, data rate, area, material budget, etc. at different experimental conditions

- Technologies for high occupancy, high radiation environments
  - Example: hybrid pixel detectors and strip detectors for the ATLAS ITk

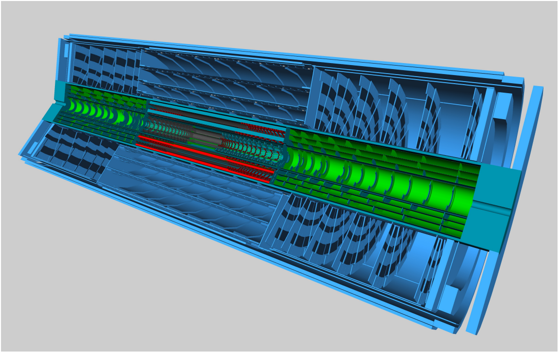
- Technologies for extremely precise tracking systems
  - Example: monolithic active pixel sensors for ALICE ITS2

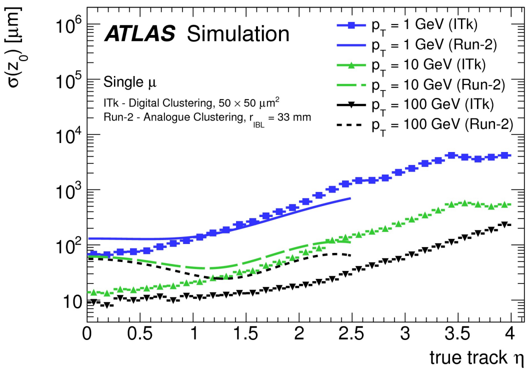
ATLAS Inner Tracker at HL-LHC*

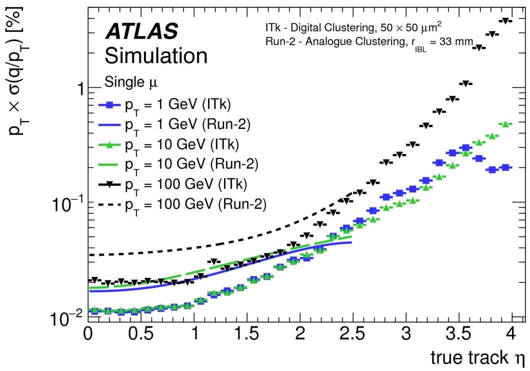
- The ATLAS ITk should have the same or better performance as the current detector but in the harsher environment of the HL-LHC
  - ⟨μ⟩ ~ 200 at 7.5×10^{34} $cm^{-2}s^{-1}$ peak luminosity
  - 4000 fb^{-1} integrated luminosity, fluences up to 2×10^{16} MeV n_{eq}/cm^2, TID up to 1 Grad



- New all-silicon detector designed using state-of-the-art silicon technologies optimised for operation in a high rate, high radiation environment
  - 13 m^2 of hybrid pixel sensors, 165 m^2 of strip sensors, 1-2% x/X_0 per layer







*The ATLAS and CMS experiments have completed R&D for their HL-LHC trackers upgrade and are starting detector production. Their upgraded trackers are thus considered state-of-the-art in this talk.

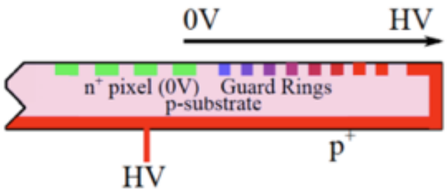
https://cds.cern.ch/record/2285585
https://cds.cern.ch/record/2257755

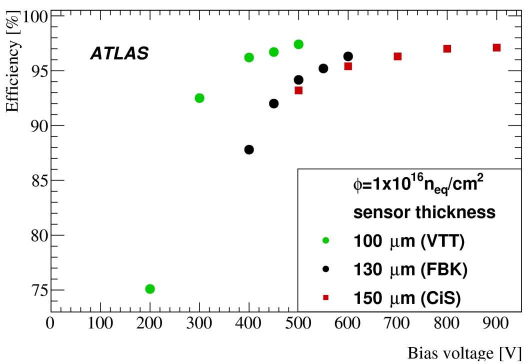
ITk pixel detector

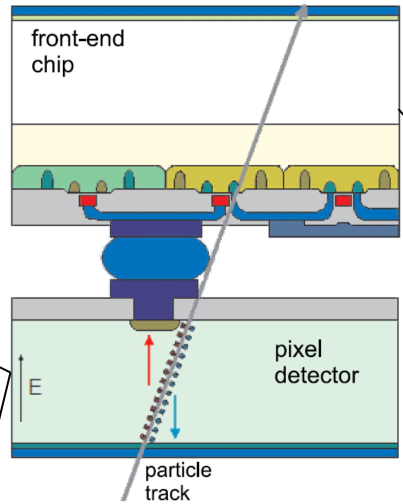
Hybrid pixel detectors: Currently the only technology that can cope with very high rate. Developed specifically for the LHC experiments. Sensor and FE are separate entities connected via fine pitch bump bonding.

Planar sensors

50x50 μm^2, 100-150 μm thin

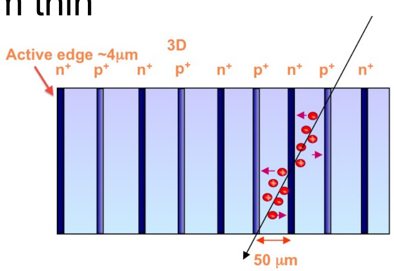


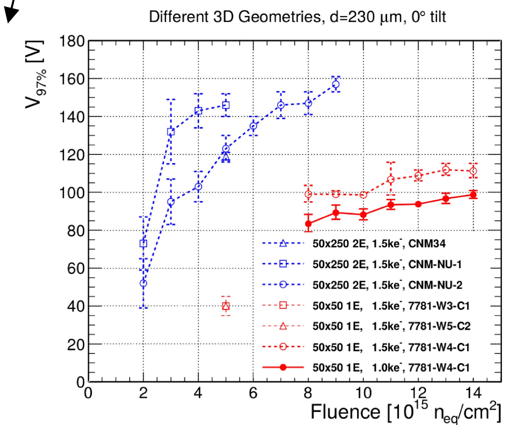




3D sensors

50x50 and 20 x 100 μm^2
150um thin

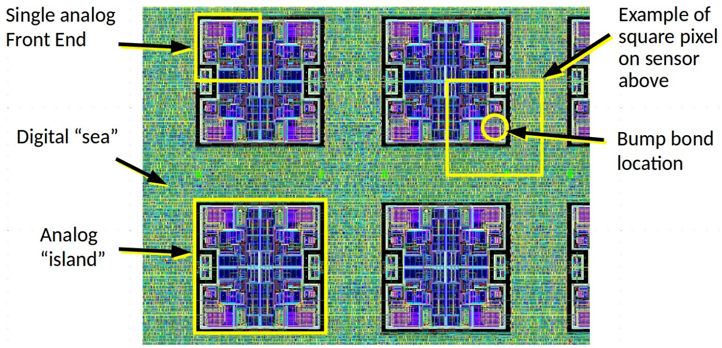




97% efficiency measured at test beams for fluence up to 1x10^{16} MeV n$_{eq}$/cm^2

FE chip

- Joint ATLAS CMS development (RD53)
- New technology node: 65 nm CMOS
- Innovative design based on a new readout architecture



Pixel size: 50x50 μm^2
Hit rate: 3GHz/cm^2
RO data rate: 5.12 Gbits/s
Rad tolerance 500Mrad at -15C
Power consumption <1W/cm^2

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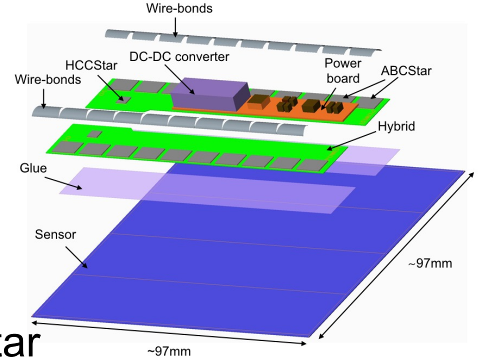
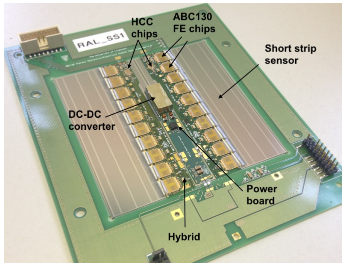
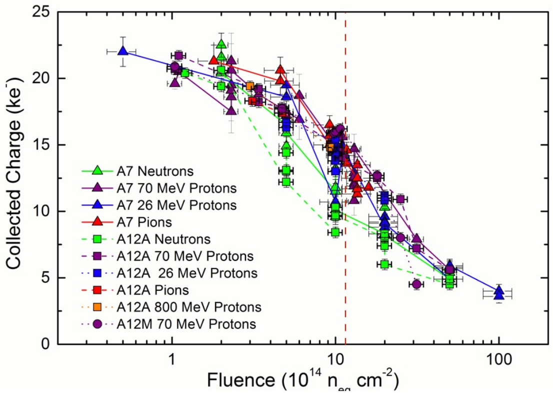
ITk strip detector

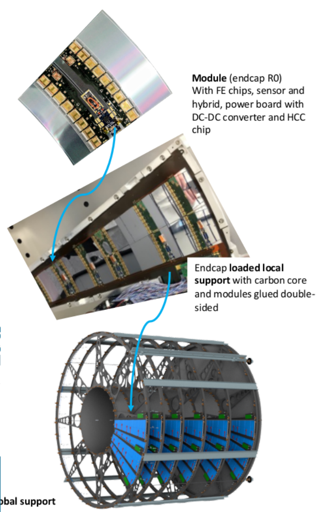




- Module = sensor + hybrid + powerboard
  - Strip pitch 75 μm, thickness 300 μm
  - Three dedicated 130 nm CMOS FE: ABCStar (readout), HCCStar (data aggregator), AMAC (power and T monitoring)
  - Design compatible with multi-level trigger scheme



- Lower data rate and radiation levels but more challenging large area production
  - Modularity of components for mass production
  - Assembly and testing at multiple sites
  - Industrialised production flow (common tooling and assembly procedures)
  - Extensive QC/QA to assure reliability in extreme experimental conditions, monitor rate and quality of production
  - Database to store QC/QA results and track components



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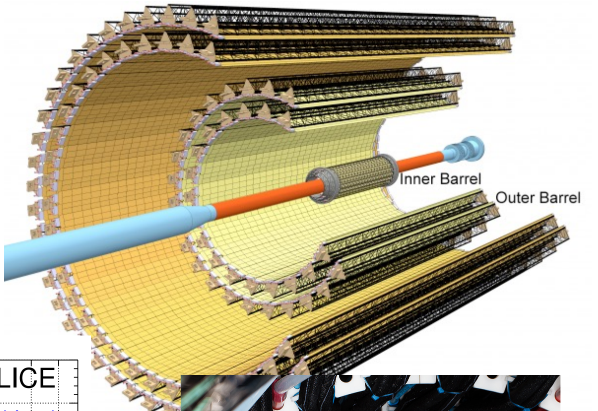
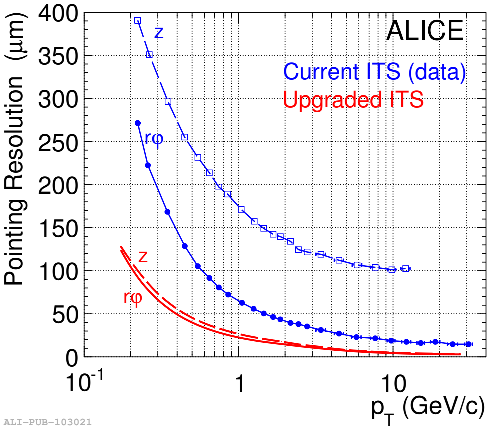
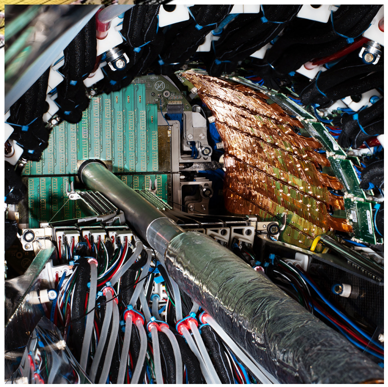
ALICE Inner Tracking System Upgrade (ITS2)

- First large-area silicon vertex detector based on the CMOS Monolithic Active Pixel Sensor (MAPS) technology optimised for extremely precise tracking
  - Sensor and electronics share the same silicon substrate
  - Small pixel pitch, very low material budget

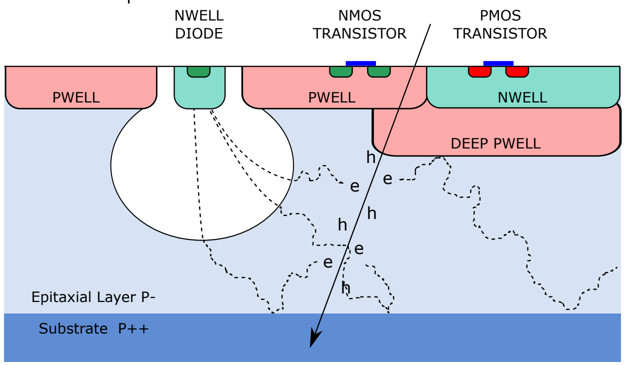


ITS2 vertex detector
7 layers, $10 m^2$, 12.5 G pixels
Innermost layer at r = 2.3 cm
Inner barrel: 0.3% x/X0
Outer barrel: 0.8% x/X0





ALPIDE sensor
180 nm TJ CMOS imaging technology
28 x 28 μm^2 pixel pitch, 50 - 100 μm thickness
Power density = 40 mW/cm^2
50 kHz interaction rate
<20 μs integration time
NIEL: 1.7 x 10^{13} 1 MeV n_{eq}/cm^2, TID: 2.7 Mrad



http://dx.doi.org/10.1016/j.nima.2015.09.057
https://arxiv.org/abs/2001.03042

Requirements for future trackers

	HL-LHC LHCb	HL-LHC ALICE 3	EIC	ILC	FCC-ee	CLIC 3TeV	FCC-hh
Fluence (n_{eq}/cm^2)	$5x10^{13}$ - $6x10^{16}$	10^{12}-10^{14}	$<10^{11}$	$<10^{10}$	$<10^{10}$	$<10^{11}$	10^{17}-10^{18}
Max hit rate ($cm^{-2}s^{-1}$)					20 M	240 k	20 G
Surface vertex (m^2)			< 1		1	1	15
Surface tracker (m^2)	26		5 - 10	150	200	140	400
Material budget per detection layer (X_0) (vertex/tracker)	≈1% ≈1%	≈0.05% ≈0.5%	≈0.05% ≈1%	≤0.2% 1 - 2%	≈0.05% ≈1%	≤0.2% ≈1%	≈1% ≤ 2 %
Position resolution vertex (μm)	≤10	≤3	≤3	≈3	≤3	≤3	≈ 7
Position resolution tracker (μm)	≈ 5	≈ 5	≈ 5	≈ 7	≈ 6	≈ 7	≈ 10
Timing resolution vertex (ns)	≤ 0.05	25		≤5	25	≈ 5	≤ 0.02
Timing resolution tracker (ns)	≤ 25	25		≤5	≤ 0.1	≤ 0.1	≤ 0.02

https://cds.cern.ch/record/2649646
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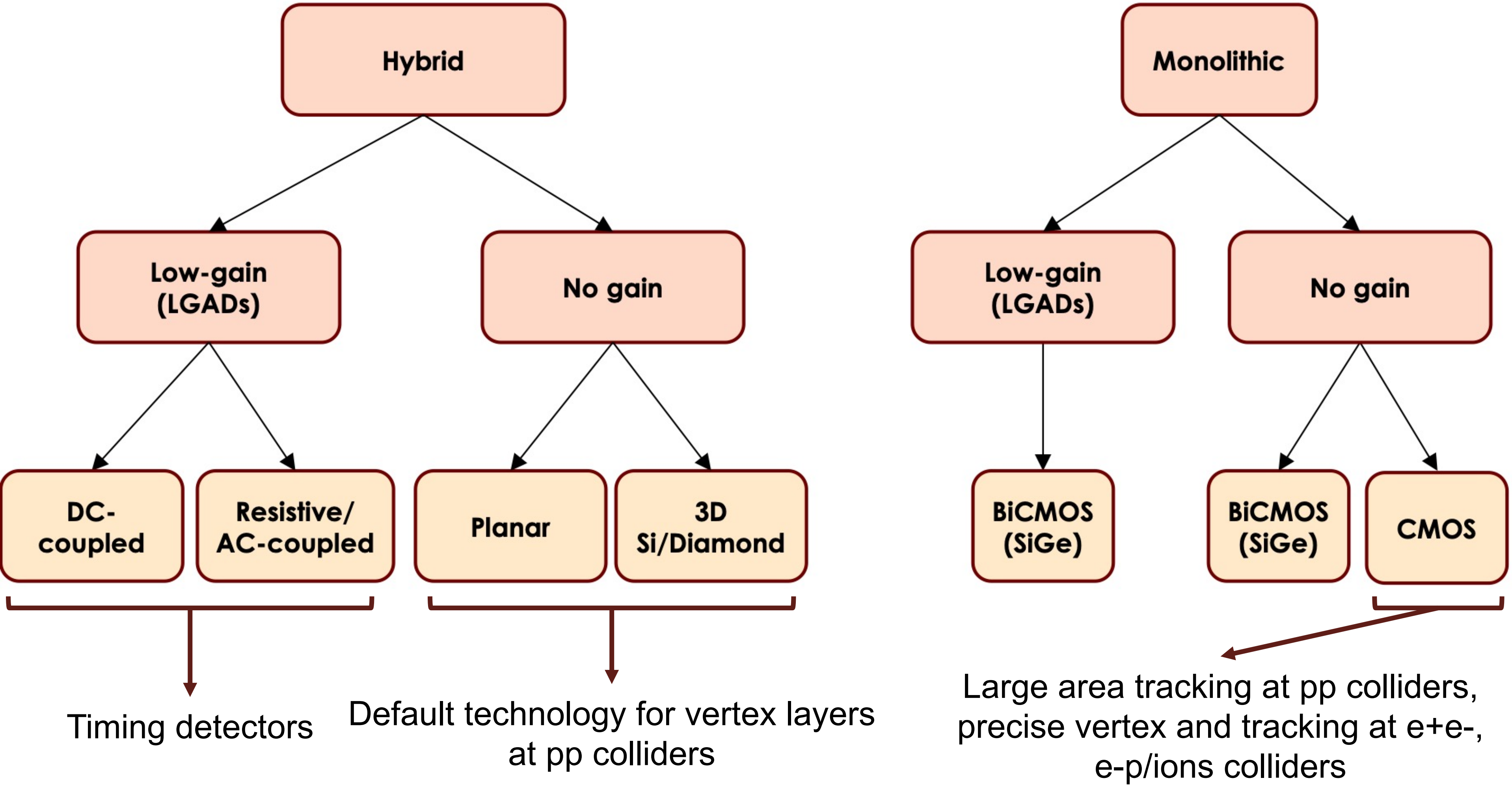
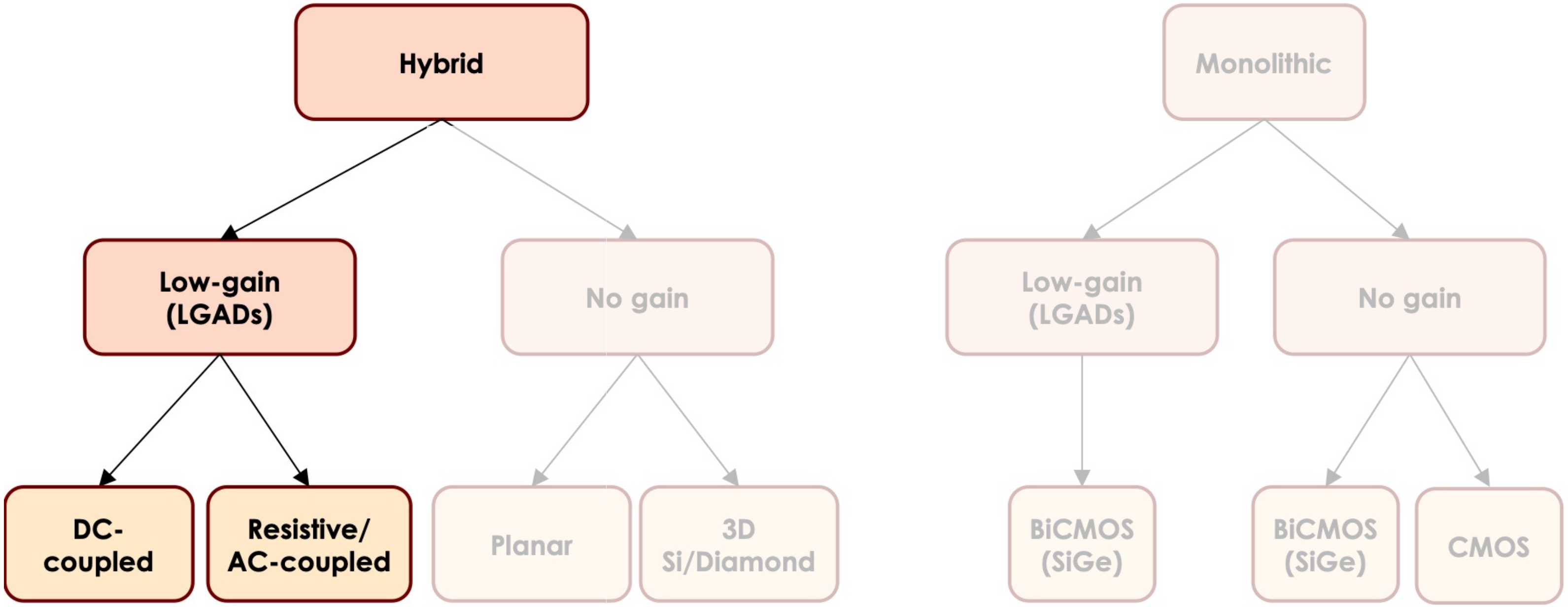
Silicon R&D for future pixel trackers



Timing detectors

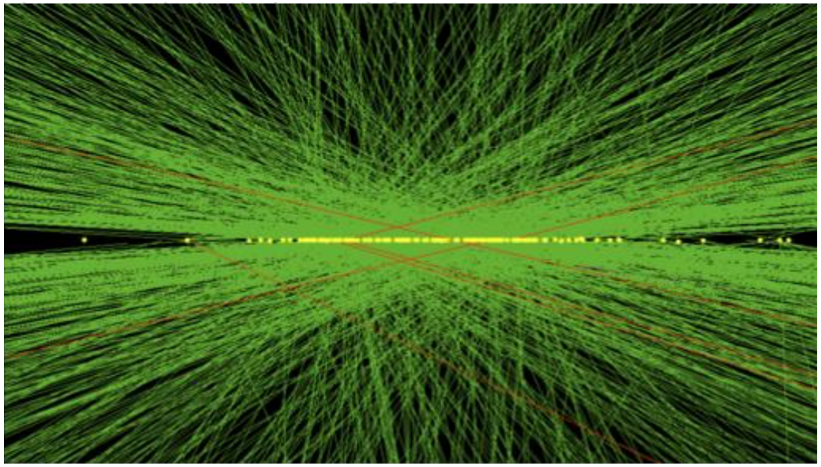


Why adding timing to 3D trackers?

- At the HL-LHC, 150-200 pile-up events per bunch crossing
  - Average distance between vertices = 500 um
  - Timing RMS spread = 150 ps

- Typical vertex separation resolution along the beam pipe 250 – 300 um

→ 10-15% of the vertices will be composed of overlapping events

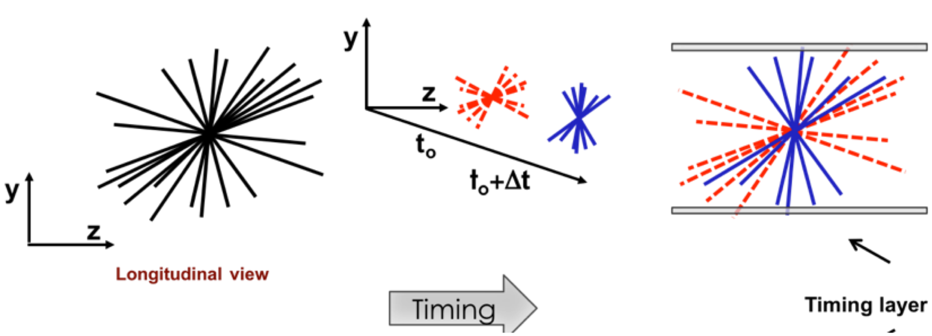


The effect of timing information

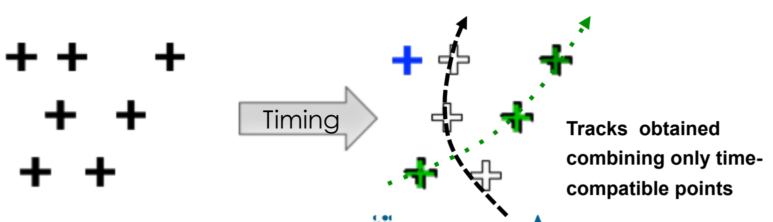
- Timing in the event reconstruction → Timing layers
  - Timing associated to each crossing track
  - Easiest implementation, only one timing layer needed
  - Overlapping events can be separated by means of an extra dimension

- Timing in track reconstruction → 4D tracking
  - Timing associated to each point along the track
  - Massive simplification of patter recognition, faster algorithms in very dense environments but massive increase of power consumption
    - Electronics needs to accurately measure timing in each pixel

Timing layers



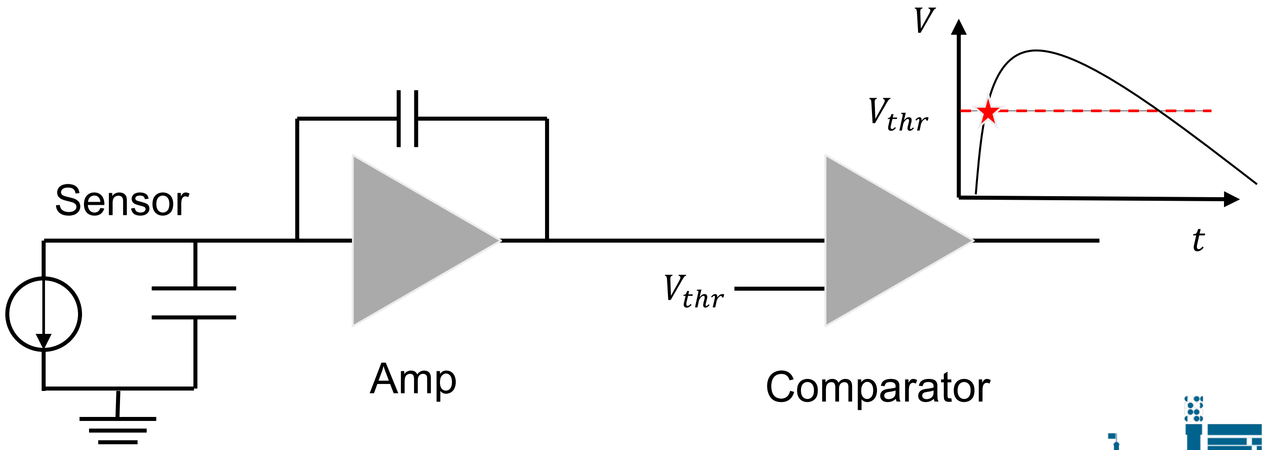
4D tracking



Time-tagging detectors

- The time resolution depends on multiple factors coming from the way the signal is generated in the sensor and then processed in the electronics
  - Time is set when the signal crosses the comparator threshold
  - A key element to good timing is uniformity of the signal

$$\sigma_t^2 = \underbrace{\sigma_{\mathrm{Land.\,TW}}^2 + \sigma_{\mathrm{Land.noise}}^2}_{\text{Physics}} + \underbrace{\sigma_{\mathrm{distorsion}}^2}_{\text{Sensor design}} + \underbrace{\sigma_{\mathrm{jitter}}^2 + \sigma_{\mathrm{TDC}}^2}_{\text{Electronics}}$$



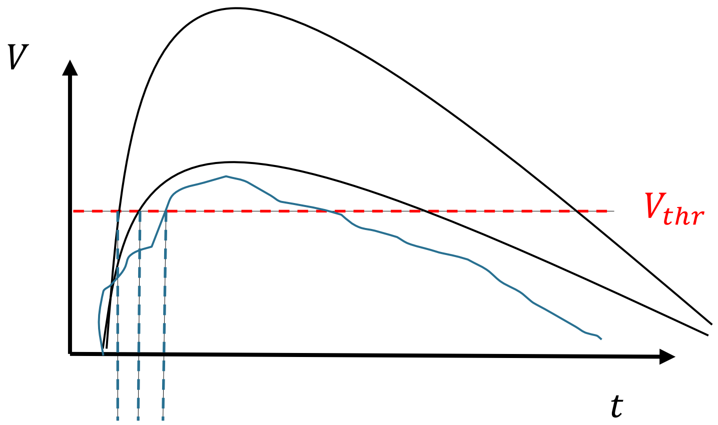
Time resolution

$$\sigma_t^2 = \sigma_{\text{Land. TW}}^2 + \sigma_{\text{Land.noise}}^2 + \sigma_{\text{distorsion}}^2 + \sigma_{\text{jitter}}^2 + \sigma_{\text{TDC}}^2$$

- Terms depending on the physics governing the energy deposition
  - The charge distribution created by a MIP in the sensor varies event-by-event (Landau distribution)

- Overall change in signal magnitude → correctable time walk
  - Appropriate electronic circuit (ToT/ToA, CDF)
  - $\sigma_{\text{Land. TW}}^2$ can be ignored

- Irregular current signal → non-correctable time walk
  - $\sigma_{\text{Land.noise}}^2$ = physical limit to the time resolution



Time resolution

$$\sigma_t^2 = \sigma_{\mathrm{Land.\,TW}}^2 + \sigma_{\mathrm{Land.noise}}^2 + \sigma_{\mathrm{distorsion}}^2 + \sigma_{\mathrm{jitter}}^2 + \sigma_{\mathrm{TDC}}^2$$

- Term depending on sensor design

- Induced current signal on the electrode given by Ramo's theorem

$$i(t) \propto q\, v_d\, E_w$$

- The drift velocity, v_d , needs to be constant in the sensor volume, otherwise variation in signal shape depending in hit position → High E-filed = saturated drift velocity
- To have uniform weighting field, E_w, width ~ pitch >> thickness
- Parallel plate sensor geometry is required for uniform v_d and E_w

Time-tagging detectors

$$\sigma_t^2 = \sigma^2_{\mathrm{Land.\ TW}} + \sigma^2_{\mathrm{Land.noise}} + \sigma^2_{\mathrm{distorsion}} + \sigma^2_{\mathrm{jitter}} + \sigma^2_{\mathrm{TDC}}$$

- Term depending on electronics

- σ^2_{TDC} : term coming from TDC binning (analogue-to-digital conversion), typically small contribution, can be ignored

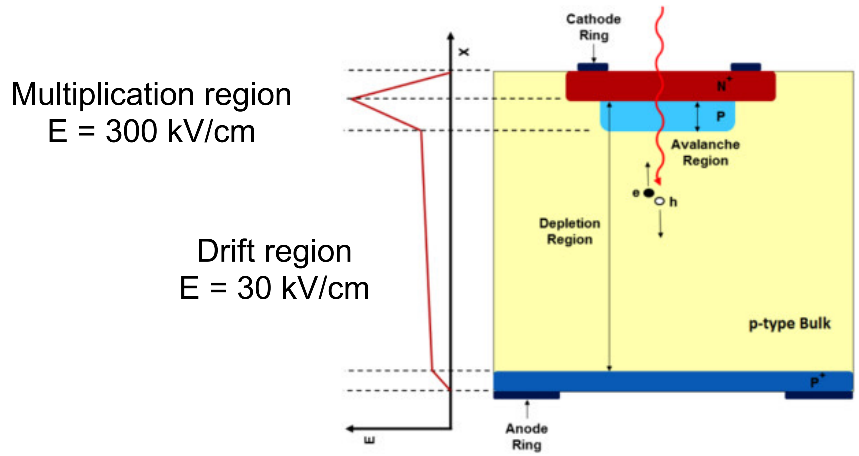
- $\sigma^2_{\mathrm{jitter}}$: mostly due to noise and the amplifier slew rate
  - Large, uniform signals
  - Low noise
  - Fast rise time

$$\sigma_{\mathrm{jitter}} \propto \frac{Noise}{dV/dT} = \frac{t_{rise}}{S/N}$$

Low Gain Avalanche Detectors (LGAD) design

1. Take a planar n-in-p sensor → Parallel plate geometry, uniform v_d and E_w
2. Add a charge multiplication layer tuned to achieve low gain → Higher S/N
3. Make the sensor thin → uniform signal, fast rise time

→ LGAD sensors produce uniform signals with low jitter



State-of-the-art LGAD for ATLAS and CMS

- Pitch: 1.3 x 1.3 mm^2
- Thickness: 50 μm
- Time resolution: ~25 ps (sensor)
- Radiation tolerance: ~ 2x10^{15} neutrons/cm^2

Established LGAD producers:
FBK, CNM, Hamamatsu
More recent additions/upcoming:
BNL, IHEP, micron, Te2V

Timing layers at ATLAS and CMS at the HL-LHC

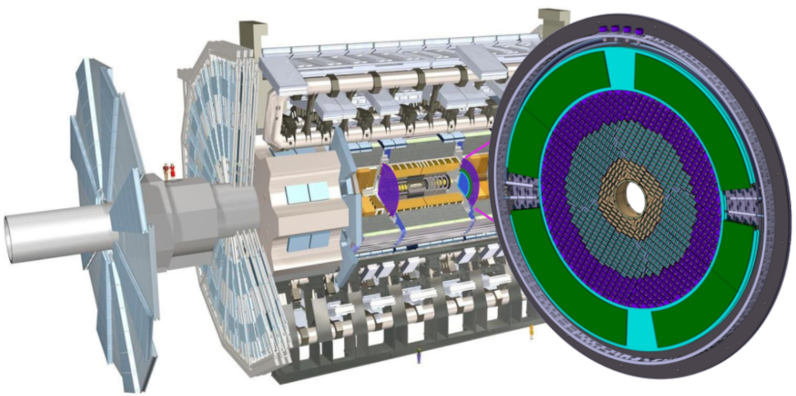
- The ATLAS and CMS timing layers will be instrumented with LGAD sensors bump bonded to dedicated readout ASICs and associated infrastructure

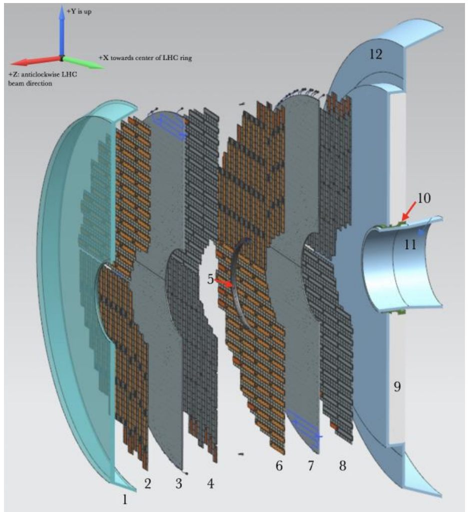
<u>ATLAS</u>

- 2 double-instrumented disks/end-cap
- Approx. 2.0 – 2.4 - 2.6 points/track
- 2.4 < |eta| < 4
- 120 mm < r < 640 mm , z = 350 cm
- 3.6M channels, 6.4 m^2

<u>CMS</u>

- 2 double-instrumented disks/end-cap
- Approx. 2 points/track
- 1.6 < |eta| < 3
- 315 mm < r < 1200 mm
- 8.5 M channels, 14 m^2





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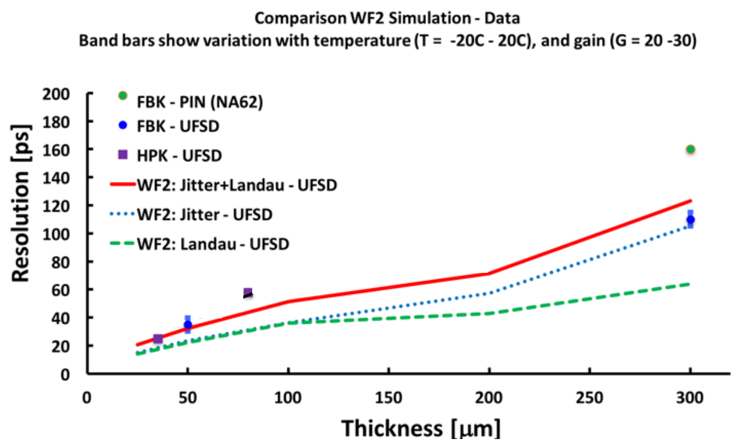
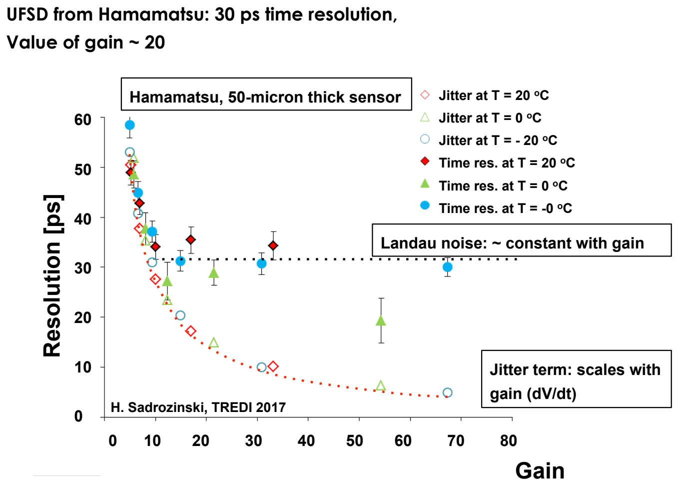
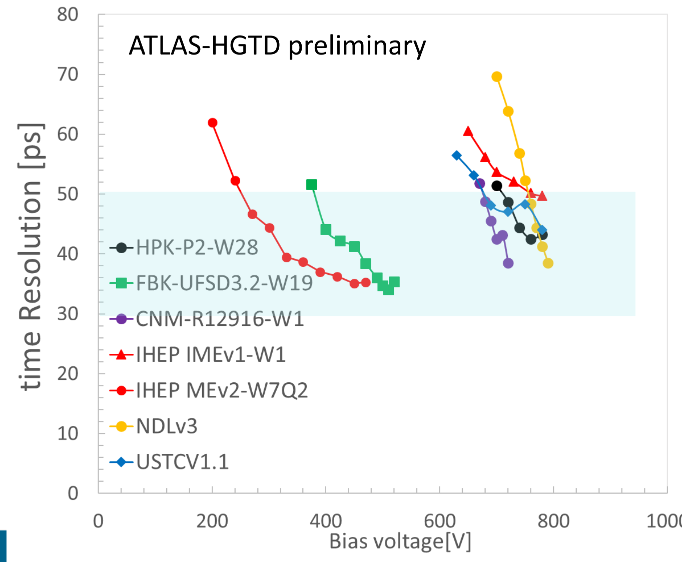
LGAD performance

- Intrinsic temporal resolution (25-30 ps) reached for thickness ≤ 50 um





- Time resolution in the 30-50 ps range at 2.5×10^{15} MeV n_{eq}/cm^2
  - C-enriched boron implants for gain layer to decrease acceptor removal



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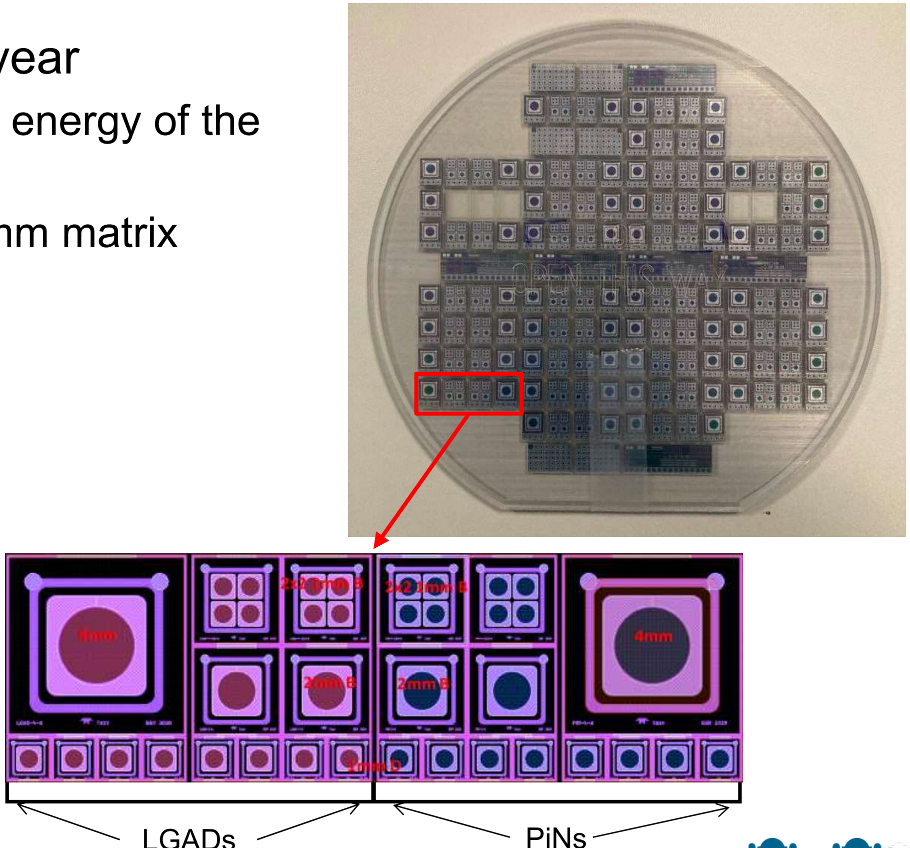
UK development with Te2v

- Collaboration between the University of Birmingham, University of Oxford, RAL and the Open University working with the UK foundry at Teledyne e2v
  - Large production volume capability as a major producer of CCDs for space, astronomy and other scientific projects
- First batch of 22 wafers produced this year
  - 8 wafer flavours with different dose and energy of the gain implant
  - 4/2/1 mm size LGADs and PIN, 2x2 2 mm matrix LGAD and PIN

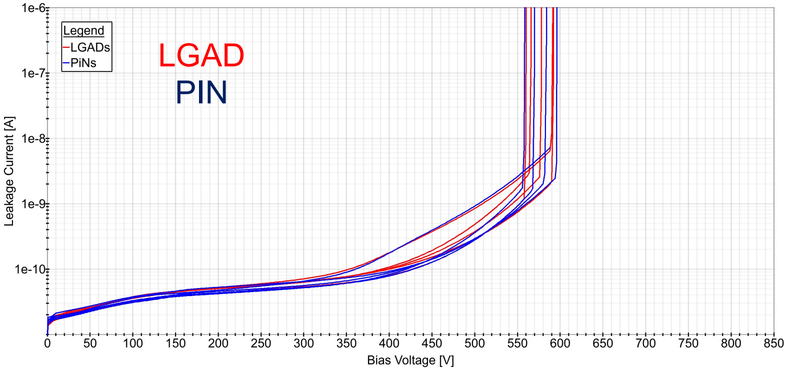
Wafer code	Normalised Dose (D)	Normalised Energy (E)
A	1.07	1.11
B	1.07	1.05
C	1.07	1.00
D	0.92	1.05
E	1.15	1.05
F	1.00	1.00
G	1.00	1.05
H	1.00	1.11



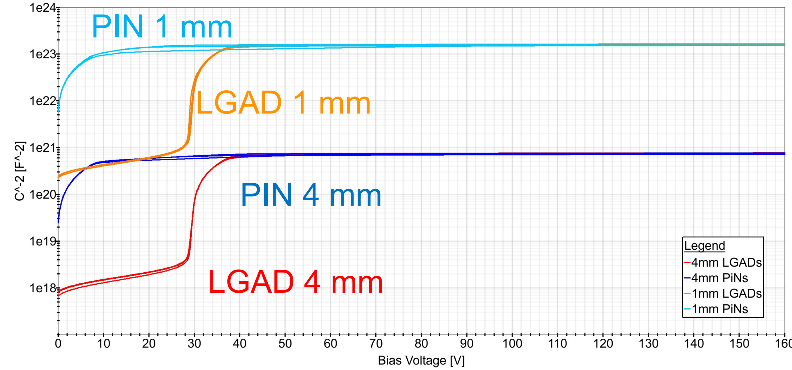
Breakdown and depletion voltages

- Extracted from IV and CV measured on wafers before dicing

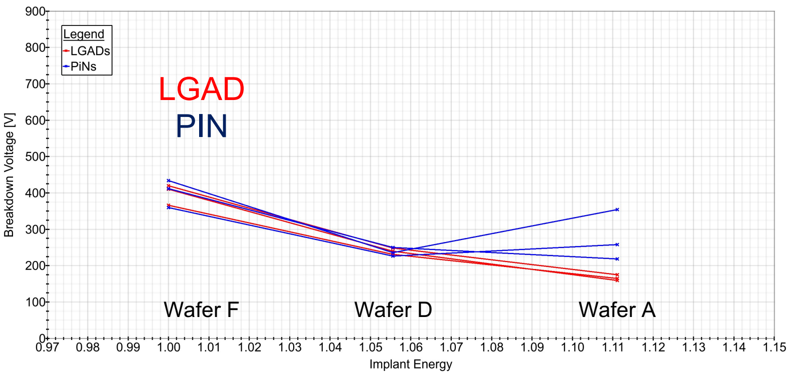
Example IV curves
Wafer F, 1 mm devices



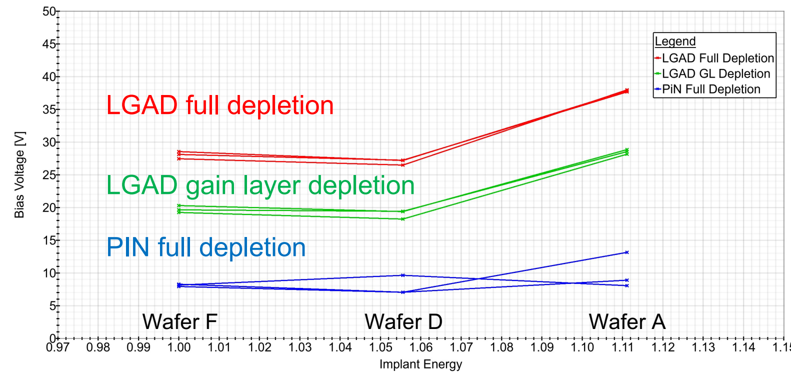
Example CV curves
Wafer A, 4 and 1 mm devices



Soft breakdown
1mm devices



Gain layer depletion and full depletion
1mm devices



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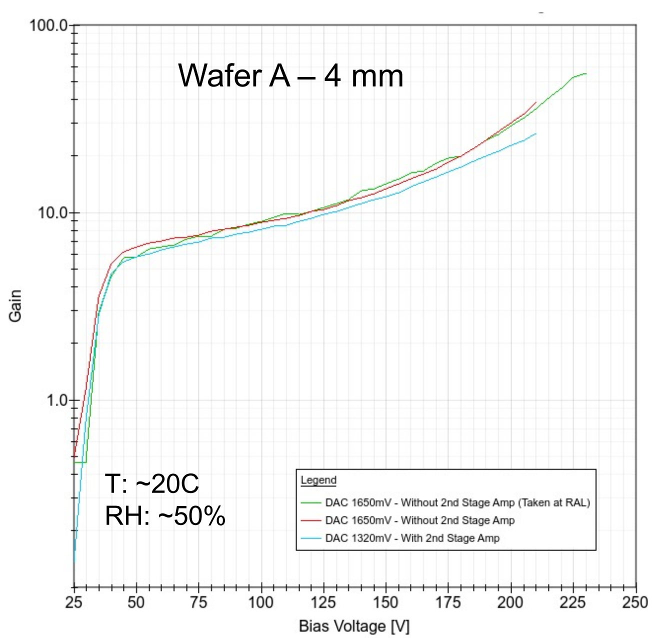
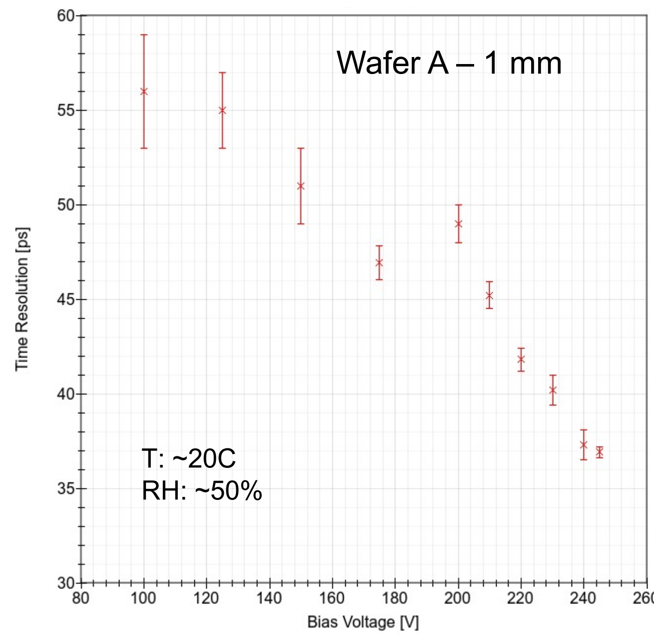
Gain and timing results before irradiation

- Gain measured with laser injection setup (1064nm IR laser)



- Time resolution measured with b-source setup



- Preliminary gain and timing performance measured on one wafer split before irradiation give results in line with those from other manufacturers
- Systematic study across wafer flavours and device size ongoing

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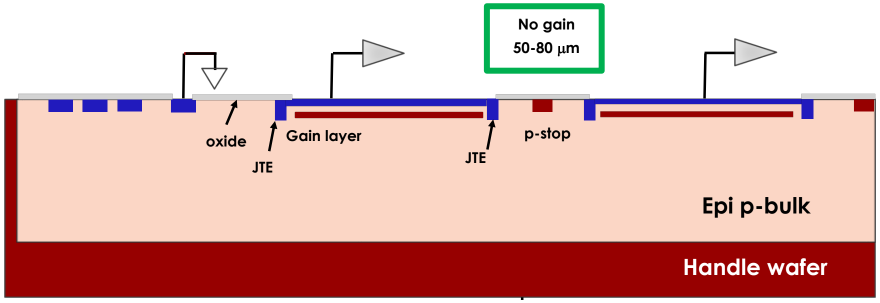
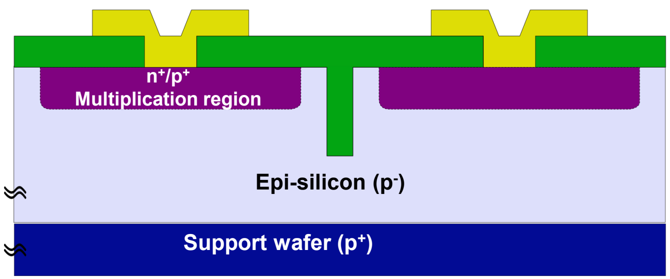
Towards 4D trackers

- LGAD shortcomings
  - Large no-gain area between pads
  - Poor spatial resolution

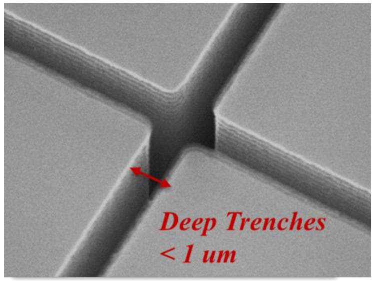


- Some small pitch developments:

<u>Trench Isolated LGAD</u>



Prototype TI-LGAD with pitch down to 50 μm; no gain region <10 μm



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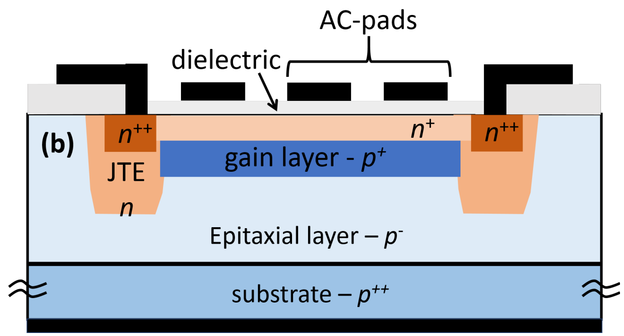
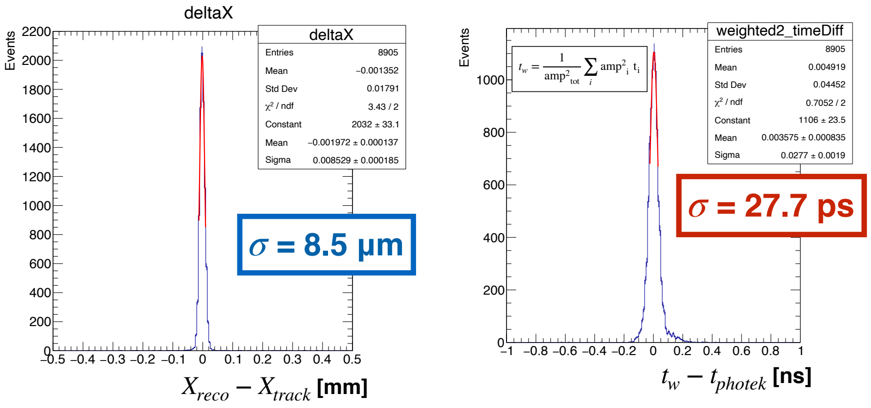
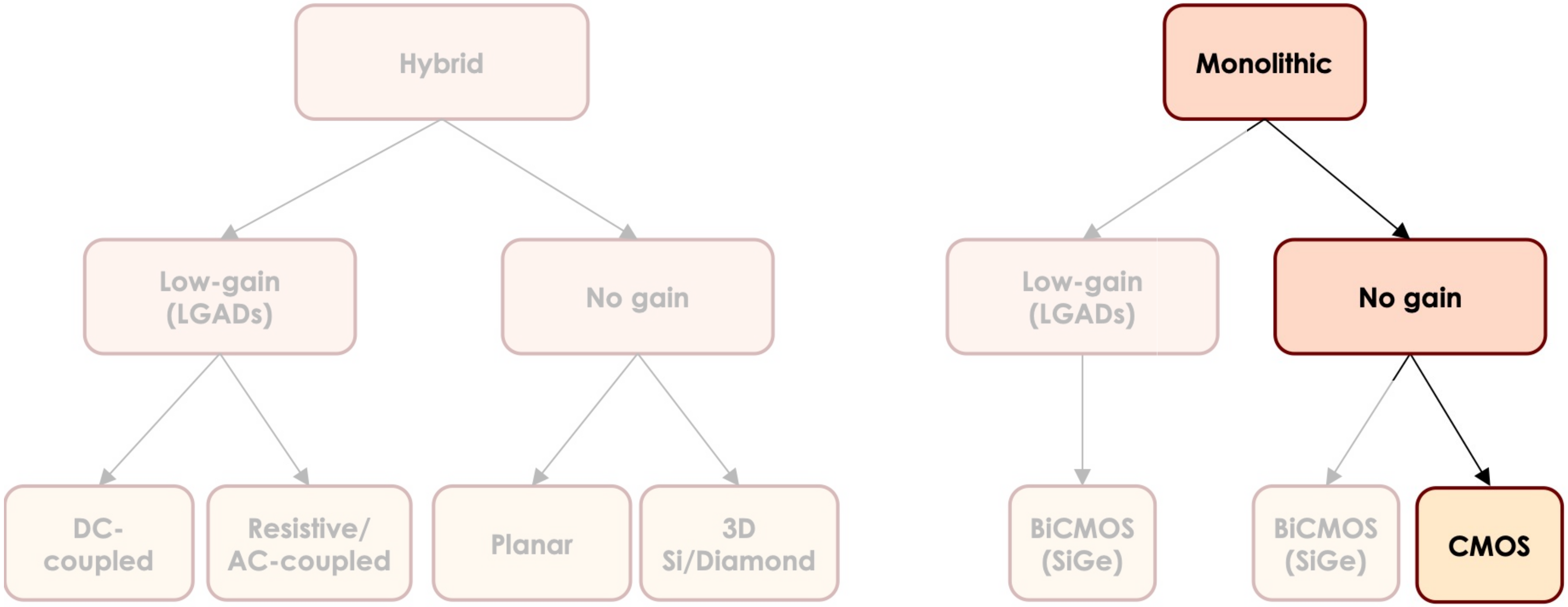
<u>AC-LGAD</u>





https://indico.cern.ch/event/1074989/contributions/4602013/

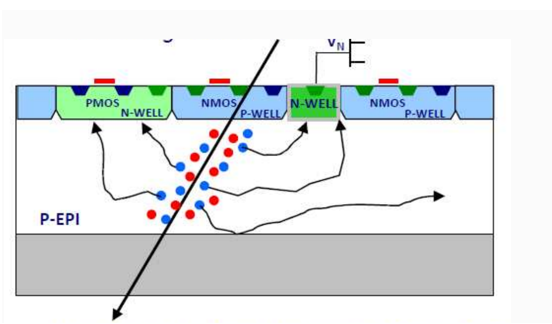
CMOS sensors

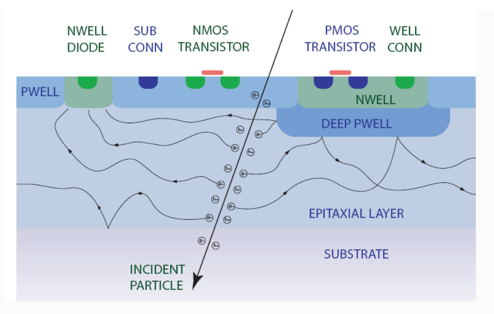


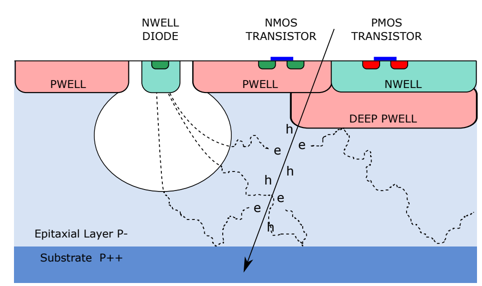
Monolithic active pixel sensors

- Traditional MAPS sensors deliver high spatial resolution through small pixel pitch and low material budget (i.e. low power consumption) and provide a simplified module concept wrt hybrids

- The ALPIDE has brought a breakthrough wrt to previous generations
  - It collects charge in part by drift → moderate rad-hard charge collection
  - It integrates full CMOS electronics → more in-pixel logic
  - It is fabricated in a commercial CMOS imaging process → low cost high volume production





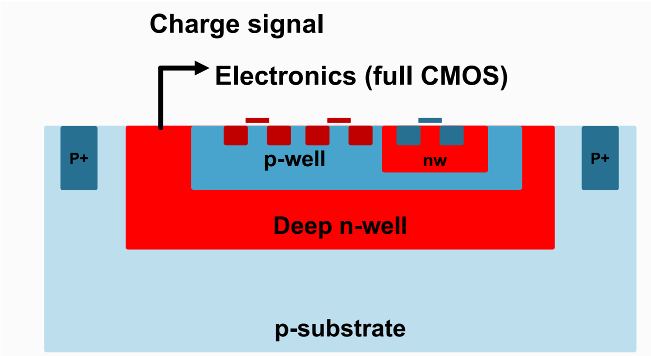


MAPS would be the perfect technology for large area trackers, but can they be made fast and radiation-hard?

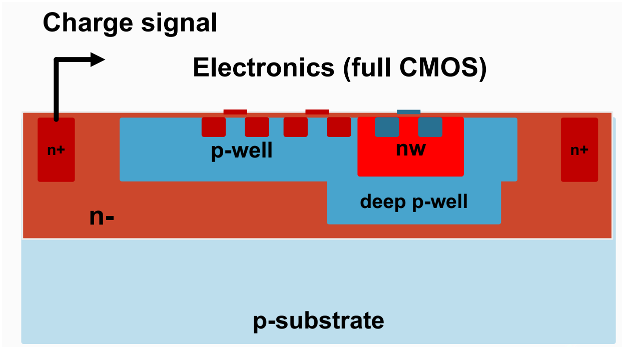
Depleted MAPS

- Fast and radiation hard charge collection requires a fully depleted sensor volume in which charges move by drift
- Need high resistivity substrates and/or being able to apply a high voltage to the sensor → This can be achieved with a number of CMOS imaging processes in particular TowerJazz and LFoundry
- Need to achieve uniform depletion = uniform electric field → requires a change in the sensor design

Large collection electrode design



Modified small collection electrode design

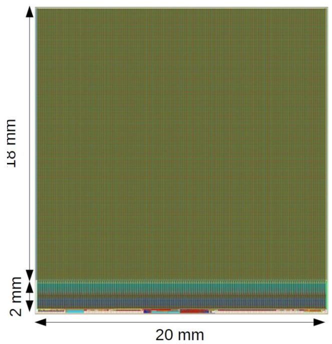


DMAPS prototypes

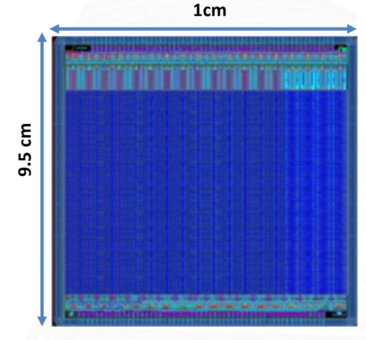
- ~ 10 years of developments led to mature prototypes of both structures that have demonstrated radiation hardness up to a few 10^{15} MeV n_{eq}/cm^2

Large collection electrode:

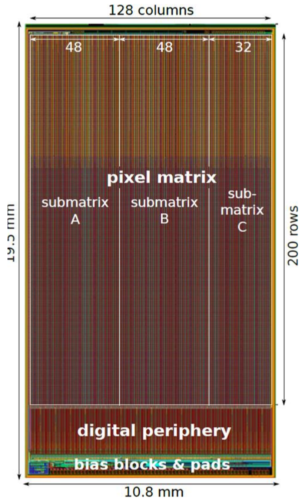
ATLASPix3 180 nm TSI



LF-MONOPIX 150 nm LFoundry

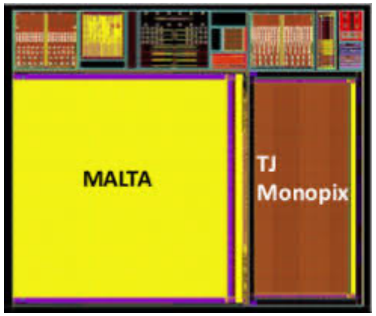


MuPix8 @ mu3e
180 nm AMS



Modified small collection electrode:

MALTA and TJ-MONOPIX
180 nm TowerJazz



… and many more, see also ARCADIA project and RD50 developments

Small collection electrode development

- The small collection electrode design has a very small detector capacitance that allows to design a compact, low power FE → small pixels and low material
  - <5fC for small electrode vs. a few hundred fC for large electrode

Estimated power consumption of ITk full scale 2x2 cm^2 DMAPS

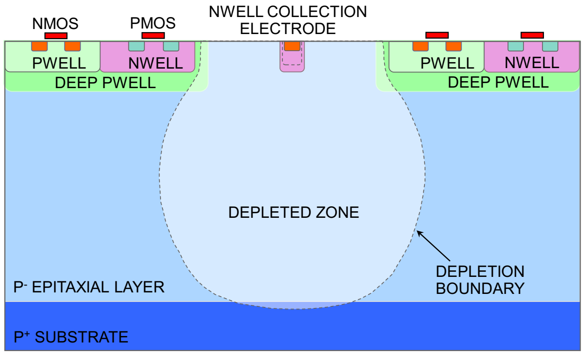
	MALTA	TJ-MONOPIX	LF-MONOPIX
Architecture	TJ Asynch.	TJ Synch.	LF Synch.
Coll. Elect.	Small	Small	Large
Pixel size	$36.4 \times 36.4\,\mu m^2$	$36.4 \times 40\,\mu m^2$	$50 \times 150\,\mu m^2$
Number of pixels	512×512	512×512	400×132
Matrix Analog Power	238 mW	238 mW	1000 mW
	($\sim$ 0.9 μW/pixel)	($\sim$ 0.9 μW/pixel)	($\sim$ 18 μW/pixel)
Matrix Digital Power	12 mW	240 mW	80 mW
	($\sim$ 0.05 μW/pixel)	($\sim$ 0.9 μW/pixel)	($\sim$ 1.5 μW/pixel)
Periphery Digital Power	267 mW	225 mW	225 mW
Total Expected Power	514 mW	703 mW	1305 mW

https://doi.org/10.1088/1748-0221/14/06/C06019

- Radiation-hardness is challenging, significant effort to develop process modifications (CERN/TJ collaboration)
- Different readout architectures explored for low power readout at high rate
  - MALTA: novel asynchronous architecture
  - TJ-MONOPIX: synchronous column drain architecture

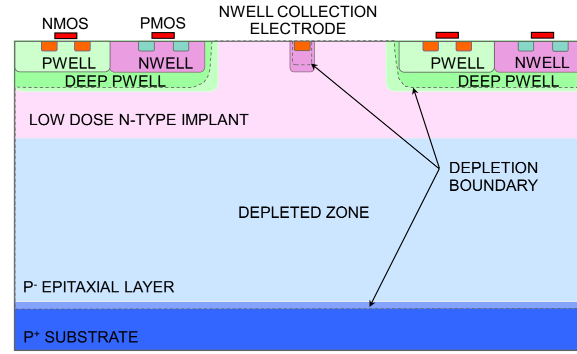
Modifications of small collection electrode design

Standard TJ 180 nm process (as in ALPIDE)

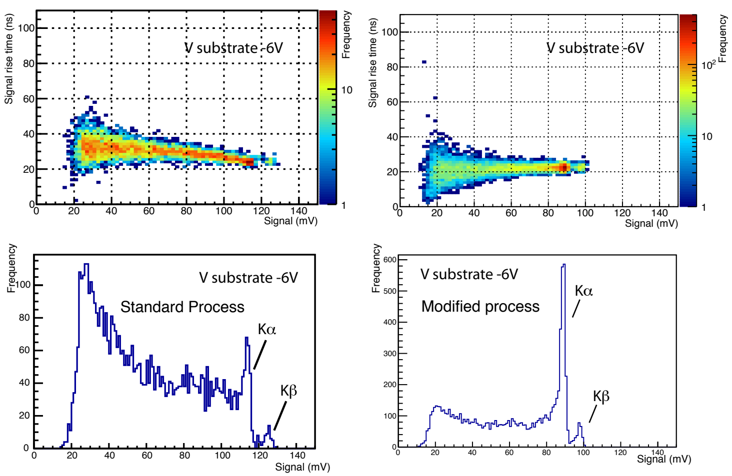


Add low dose n-implant to improve depletion under deep p-well

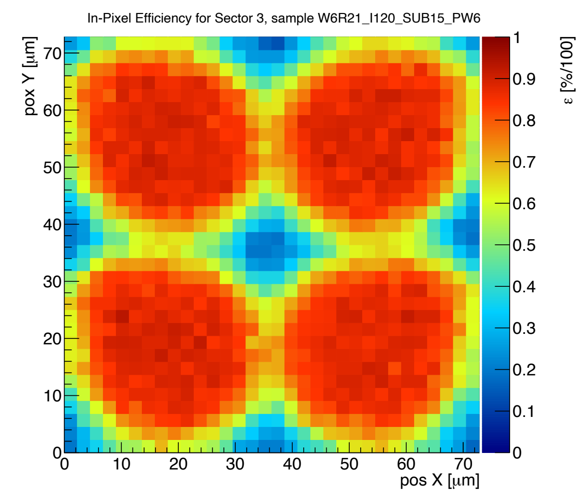
Modified TJ 180 nm process



Results on pixel test structures (TJ investigator) indicated larger depletion



Efficiency for the first MALTA prototype measured in a 180 GeV proton beam (2018) – Degradation at pixel edges after 10^{14} n_{eq}/cm^2

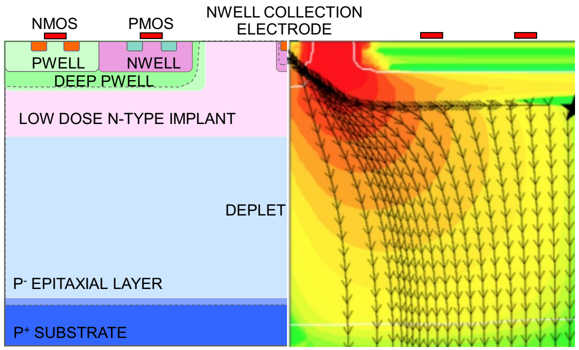


http://dx.doi.org/10.1016/j.nima.2017.07.046
https://doi.org/10.1088/1748-0221/14/05/C05013
https://doi.org/10.1016/j.nima.2019.162404

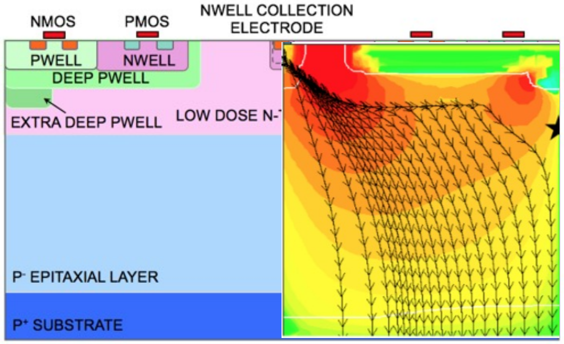
Modifications of small collection electrode design

- Further modifications needed to improve lateral field strength

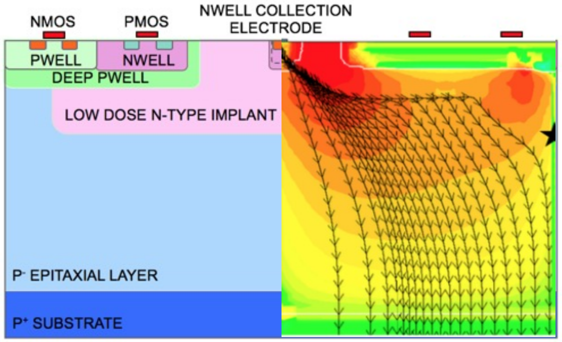
Modified



Modified extra deep pwell

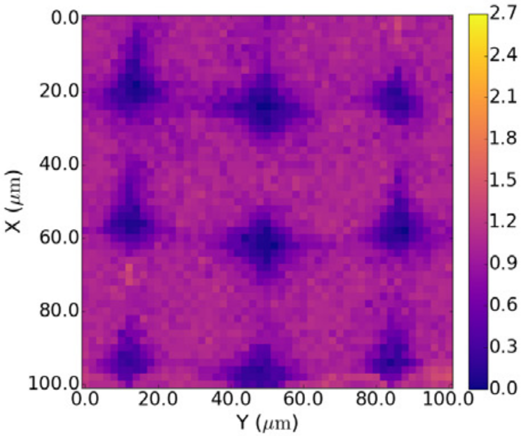


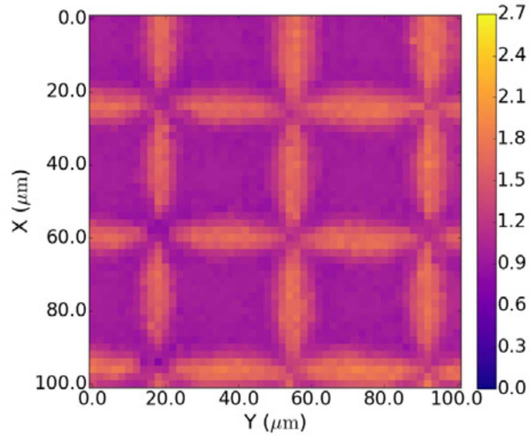
Modified n-gap

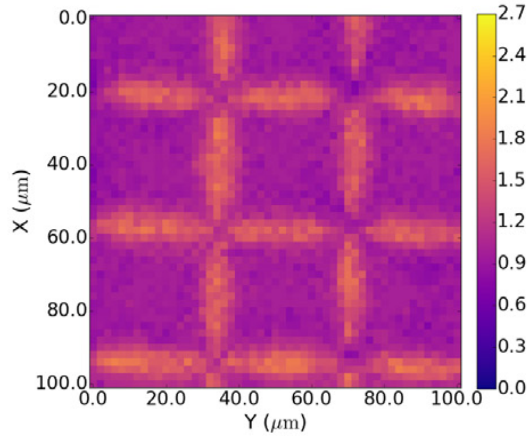


- Mini-MALTA pixel sectors with different sensor modifications tested with a x-ray beam at the Diamon Light Source (2019) demonstrate improved response at pixel edges after $1x10^{15}$ n_{eq}/cm^2

https://doi.org/10.1016/j.nima.2019.163381



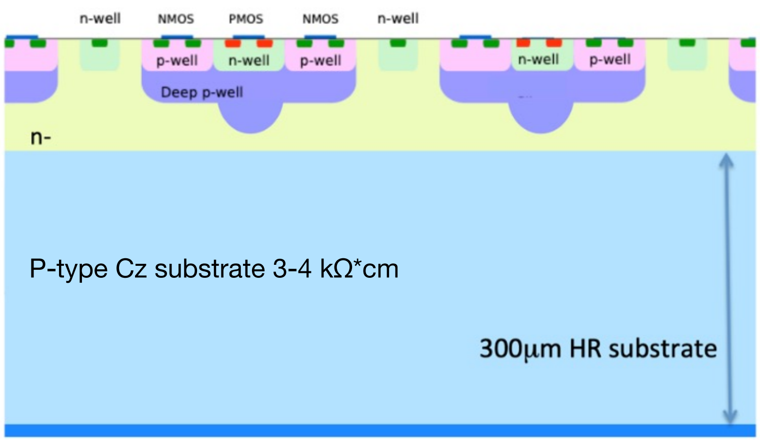


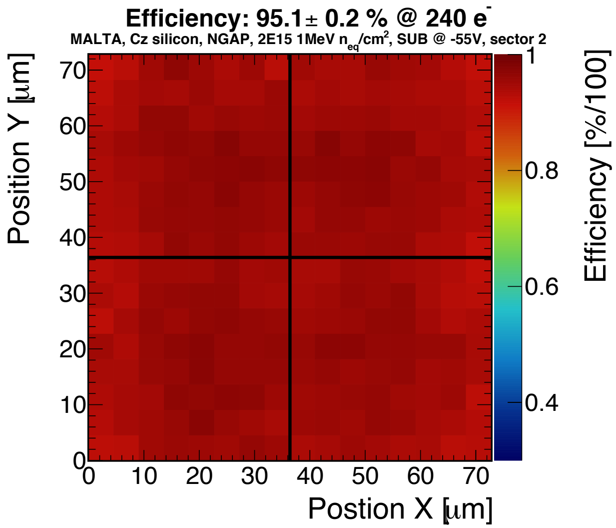


Modifications of small collection electrode design

- One of the most recent MALTA version has been implemented on high resistivity Czochralski substrate
  - Resistivity and bias voltage higher than for epitaxial layer in previous prototypes
  - Implemented with modified, n-gap, deep p-well modifications
  - Higher charge collection, time resolution, radiation hardness expected

- MALTA Cz sensors allow further depletion than epitaxial layers
  - Corner efficiency after $2x10^{15}$ n_{eq}/cm^2 fully recovered with extra process modification measured at DESY test beam 4 GeV electron beam (2019)





https://indico.cern.ch/event/1047531/contributions/4521226/

Next generation MAPS: 65 nm CMOS sensors

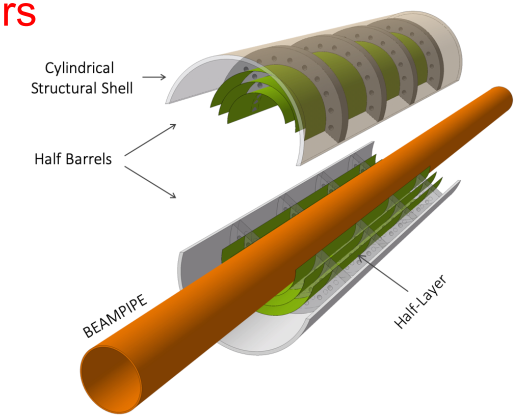
- DMAPS in 150/180nm CMOS imaging processes are approaching HL-LHC rate capability and radiation hardness
  - Candidates for ATLAS inner vertex layers replacement after 2030

- Future facilities present bigger challenges → explore smaller feature size technology

- R&D is starting to develop MAPS in 65 nm CMOS imaging process for use at future collider facilities
  - Higher logic density (increased performance/area, higher granularity)
  - Lower power
  - Higher speed (logic, data transmission…)
  - Process availability
  - Higher NRE costs and complexity, but lower price per area

Ongoing 65 nm R&D for ALICE ITS3 vertex detector

- New generation MAPS sensor at the 65 nm node to design a truly cylindrical, extremely low mass (0.05% x/X0) vertex detector (~0.12m^2) for the HL-LHC (after 2030)
  - Exploit stitching over large area to design wafer scale sensors
  - Thin sensors bent around the beam pipe
  - Lower power in 65 nm allows air cooling
  - Minimal support needed and services outside active area



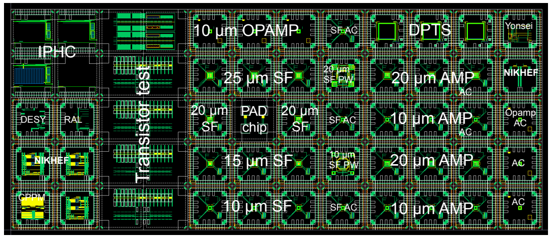
ALICE

Specifications

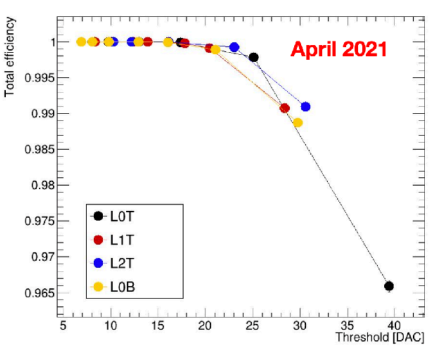
Parameter	ALPIDE (existing)	Wafer-scale sensor (this proposal)
Technology node	180 nm	65 nm
Silicon thickness	50 µm	20-40 µm
Pixel size	27 x 29 µm	O(10 x 10 µm)
Chip dimensions	1.5 x 3.0 cm	scalable up to 28 x 10 cm
Front-end pulse duration	~ 5 µs	~ 200 ns
Time resolution	~ 1 µs	< 100 ns (option: <10ns)
Max particle fluence	100 MHz/cm^2	100 MHz/cm^2
Max particle readout rate	10 MHz/cm^2	100 MHz/cm^2
Power Consumption	40 mW/cm^2	< 20 mW/cm^2 (pixel matrix)
Detection efficiency	> 99%	> 99%
Fake hit rate	< 10^{-7} event/pixel	< 10^{-7} event/pixel
NIEL radiation tolerance	~3 x 10^{13} 1 MeV n_{eq}/cm^2	10^{14} 1 MeV n_{eq}/cm^2
TID radiation tolerance	3 MRad	10 MRad

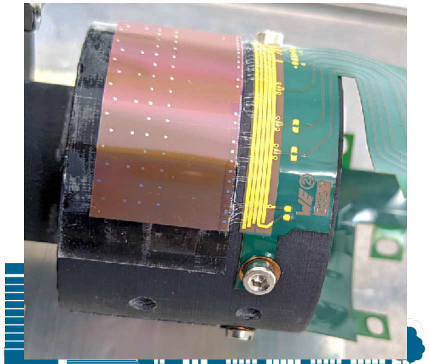
M. Mager | ITS3 kickoff | 04.12.2019

First submission in TJ 65 nm within CERN EP R&D WP1.2



Efficiency versus bending radii with bent ALPIDE (test beam data)





- The EIC plans to use the same sensor for its vertex and tracking detector

https://cds.cern.ch/record/2644611
https://arxiv.org/abs/2105.13000
https://indico.cern.ch/event/1071914/

Conclusion

- Silicon detectors are the only technology that can satisfy the requirements of vertex and tracking detectors at collider experiments

- A large R&D programme is ongoing to further improve their performance to match the challenges of future applications

- The addition of high time precision to the fine granularity of pixel detectors is the key innovation for tracking at high luminosity colliders

- Recent and new developments in CMOS sensors will provide the breakthrough technology for future vertex and tracking matching the requirements of most applications

Backup